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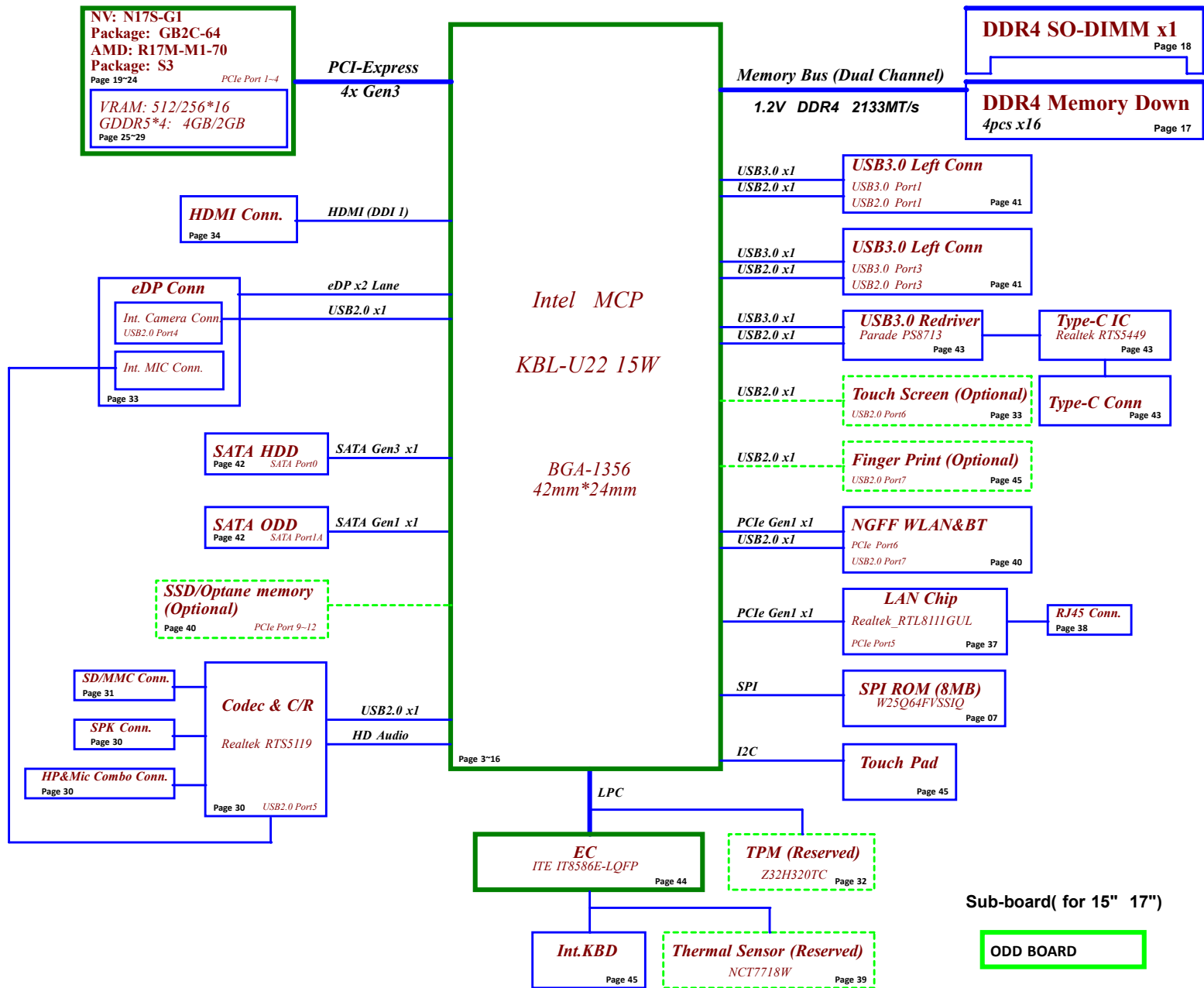
EG523 MB Schematics Document

Kabylake-U42 with DDR4 + AMD R17M-M1-70 GPU with GDDR5

2017-03-15

REV: 0.1

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Cover Page			
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane				
State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

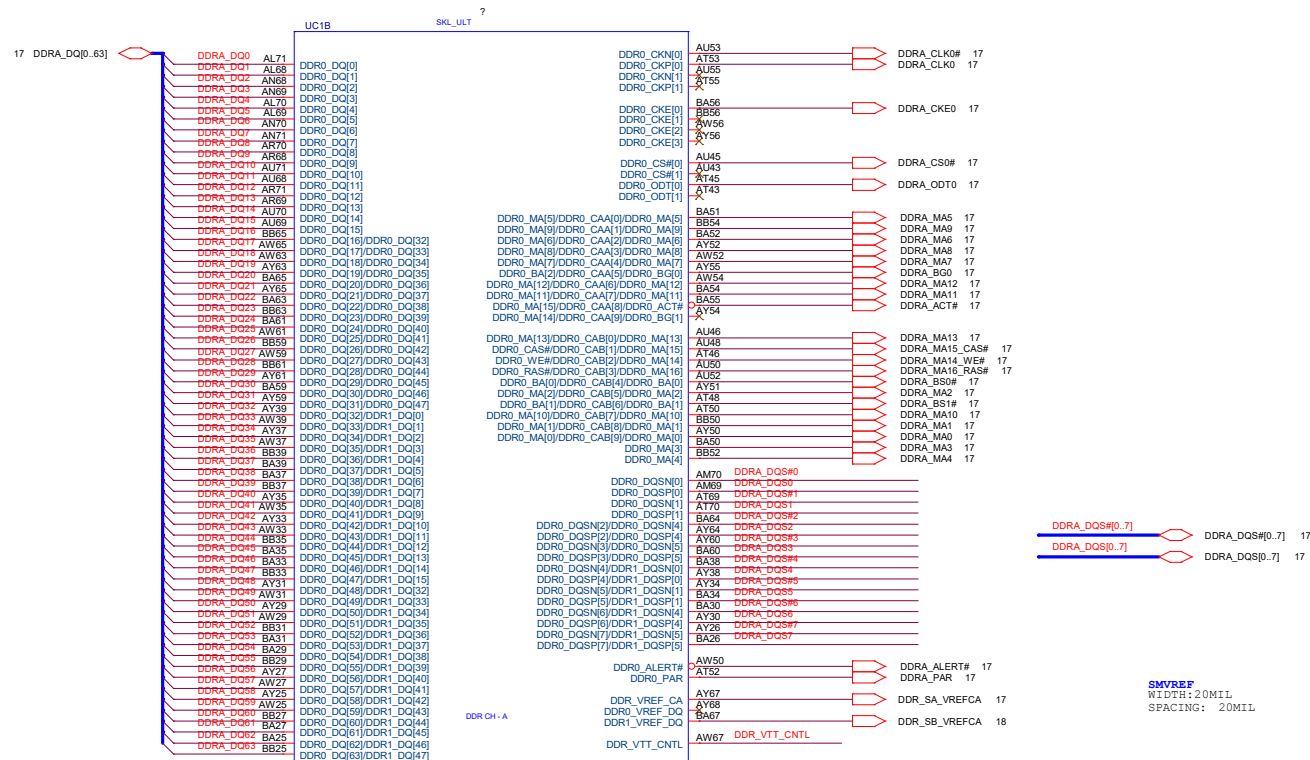
EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	DDR4 SODIMM	need to update	Wlan	need to update
Charger	0001 0010 b	PCH	need to update				
		DGPU	need to update				

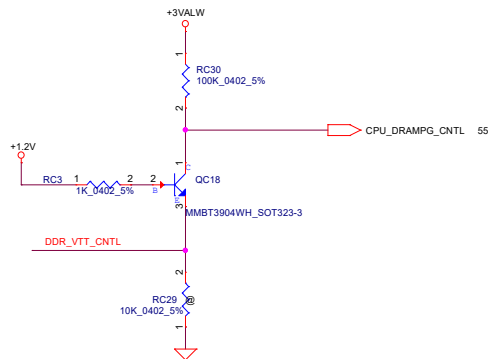
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF


HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB Type-C
	3	USB3.0 Conn Left
	4	Finger Print
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	Camera
	9	NC
	10	NC
PCIE	1~4 X4 PCIE	DGPU
	5	LAN
	6	WLAN
	7	SATA HDD
	8	SATA ODD
	9~12 X4 PCIE	Optane Memory
	0	HDD
	1A	ODD
SATA	1B	used as PCIE
	2	used as PCIE

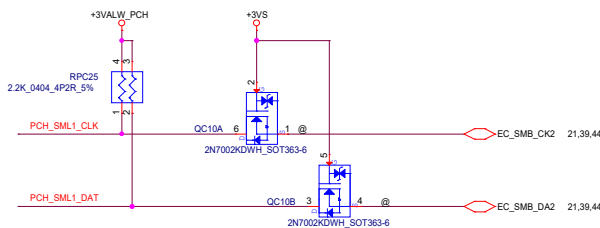
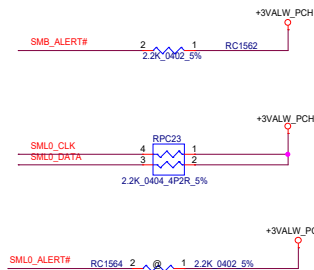
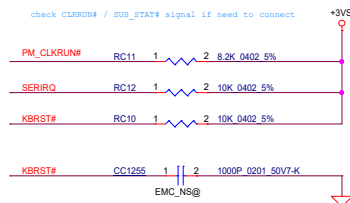
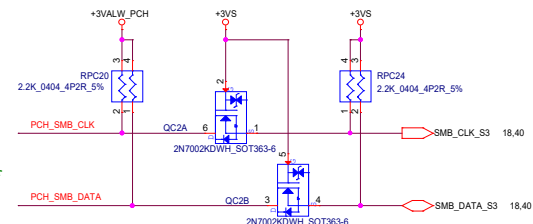
BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part



SKYLAKE-U_BGA1356
REV = 1
@



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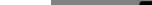
This signal has a weak internal pull-down.
0 = LPC is selected for EC. (Default)
1 = eSPI is selected for EC.

Notes:

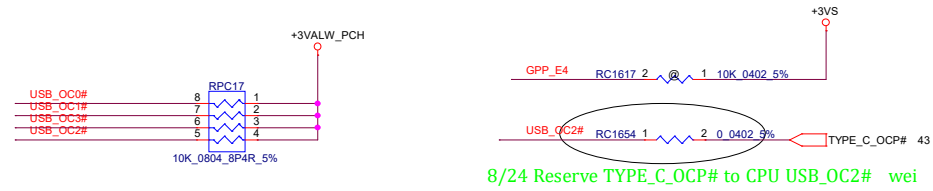
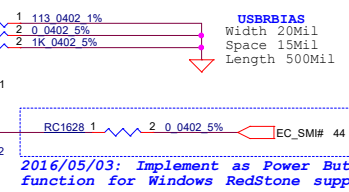
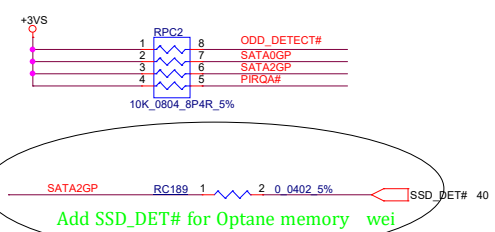
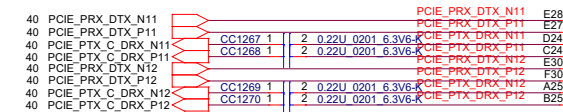
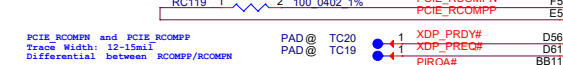
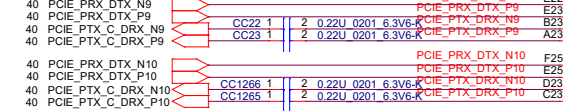
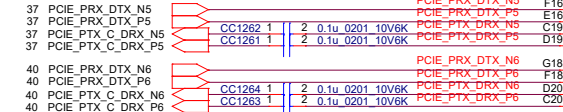
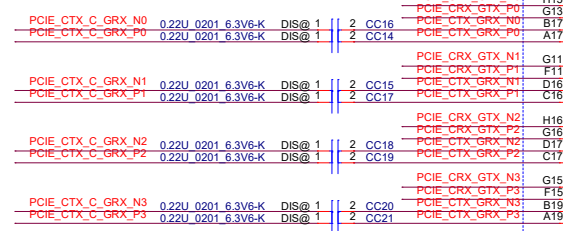
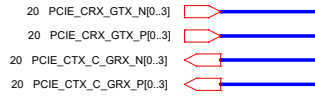
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary welf Rising edge of RSMRST#




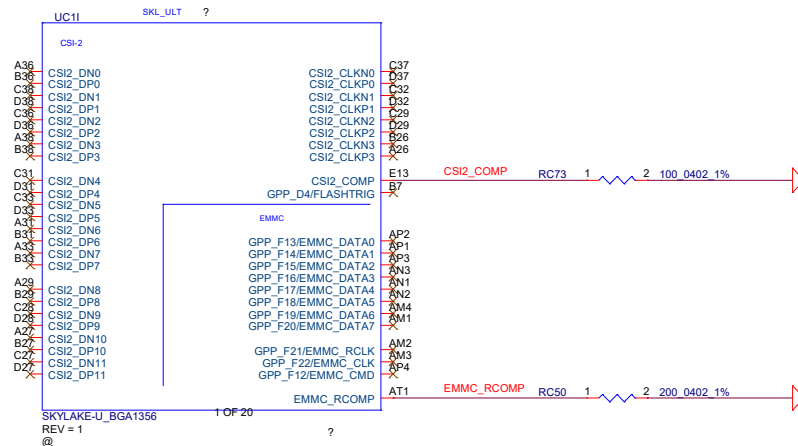
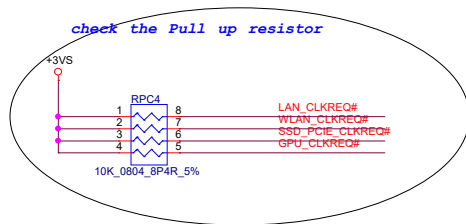
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@DIS For NV and AMD GPU SKU



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@DIS For NV and AMD GPU SKU

PCIE CLK0 DGPU

20 CLK_PCIE_GPU#
20 CLK_PCIE_GPU#
21 GPU_CLKREQ#

CLK_PCIE_GPU# D42
CLK_PCIE_GPU# C42
GPU_CLKREQ# AR10

Optane memory

40 CLK_PCIE_SSD#
40 CLK_PCIE_SSD
40 SSD_PCIE_CLKREQ#

CLK_PCIE_SSD# B42
CLK_PCIE_SSD A42
SSD_PCIE_CLKREQ# AT7

PCIE CLK5 WLAN

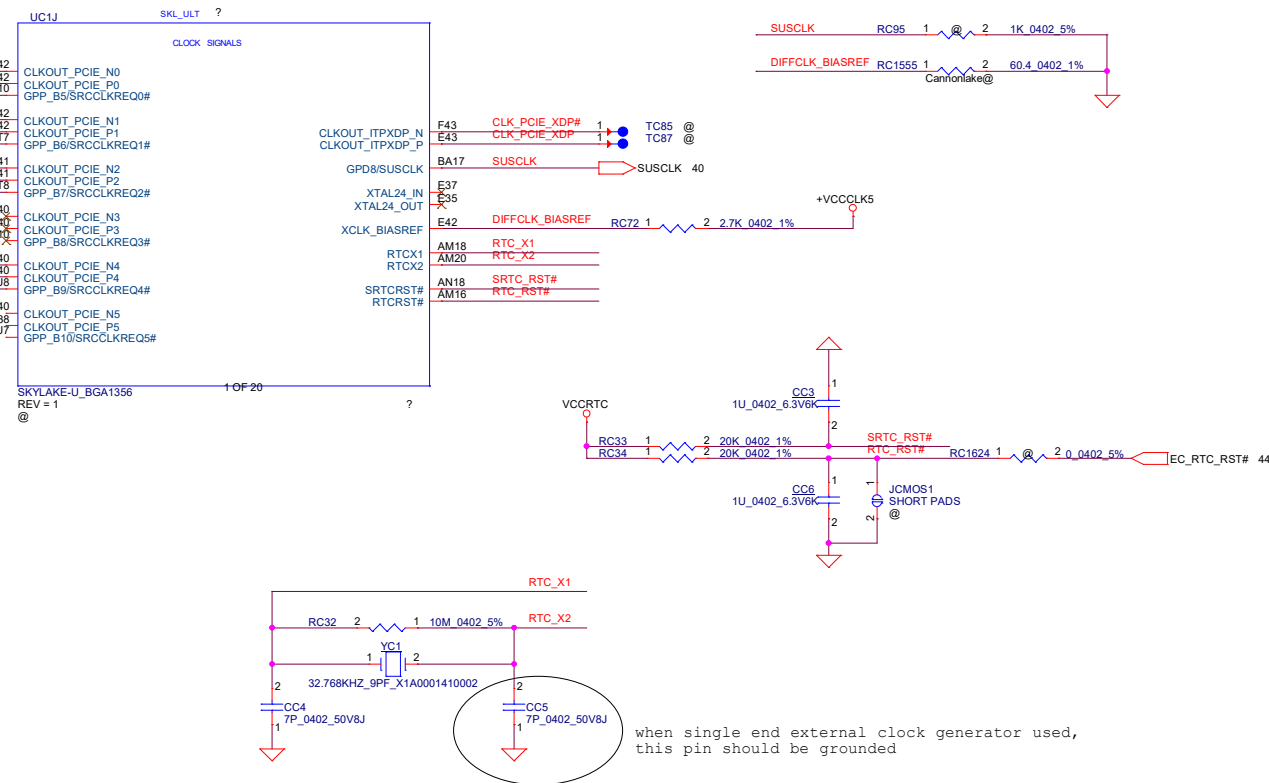
40 CLK_PCIE_WLAN#
40 CLK_PCIE_WLAN
40 WLAN_CLKREQ#


CLK_PCIE_WLAN# D41
CLK_PCIE_WLAN C41
WLAN_CLKREQ# AT8

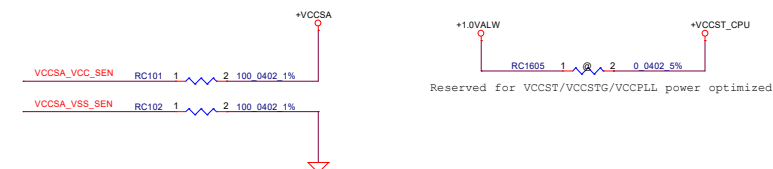
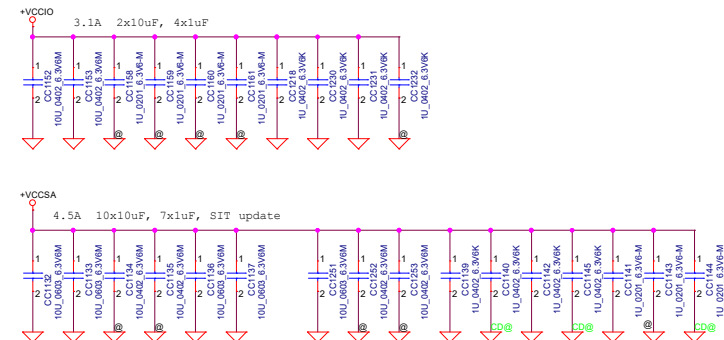
PCIE CLK4 LAN


37 CLK_PCIE_LAN#
37 CLK_PCIE_LAN
37 LAN_CLKREQ#

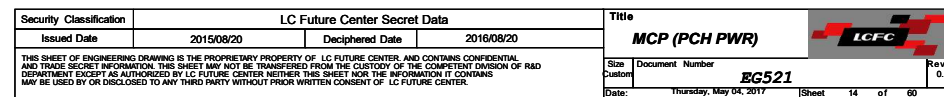
CLK_PCIE_LAN# B40
CLK_PCIE_LAN A40
LAN_CLKREQ# AU6

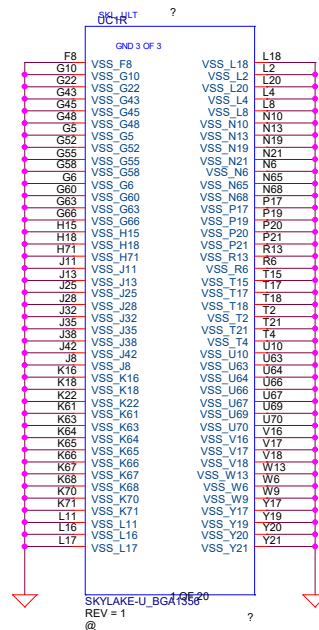
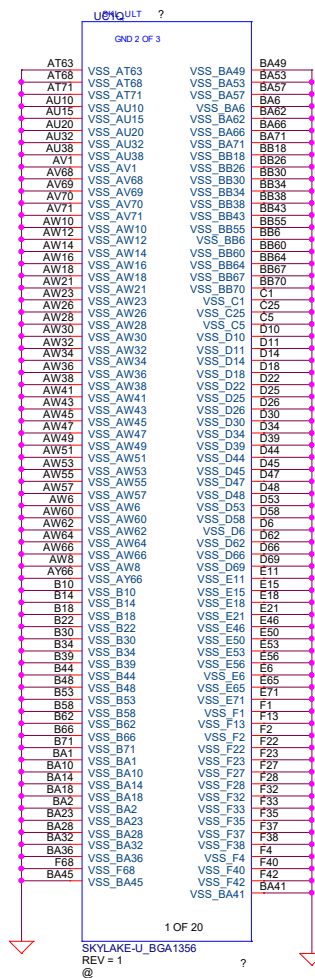
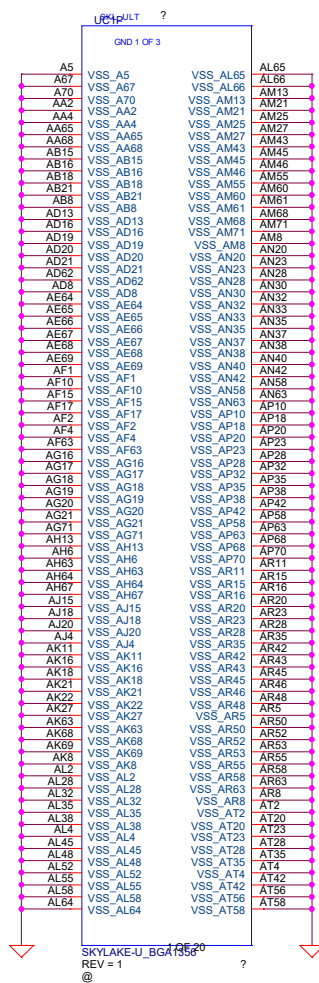


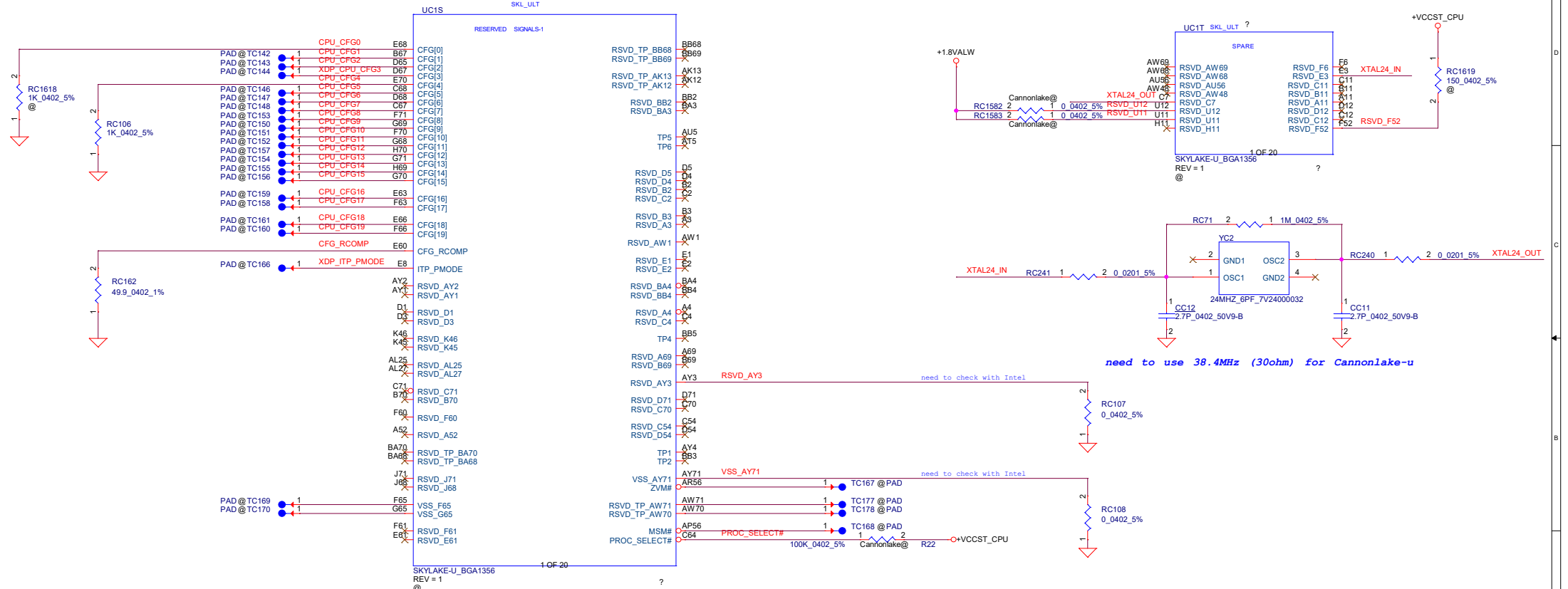
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Issued Date	2016/12/14	Deciphered Date	2017/12/13	MCP (CSI2,EMMC,CLOCK) 	
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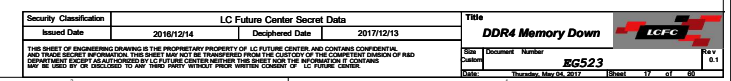




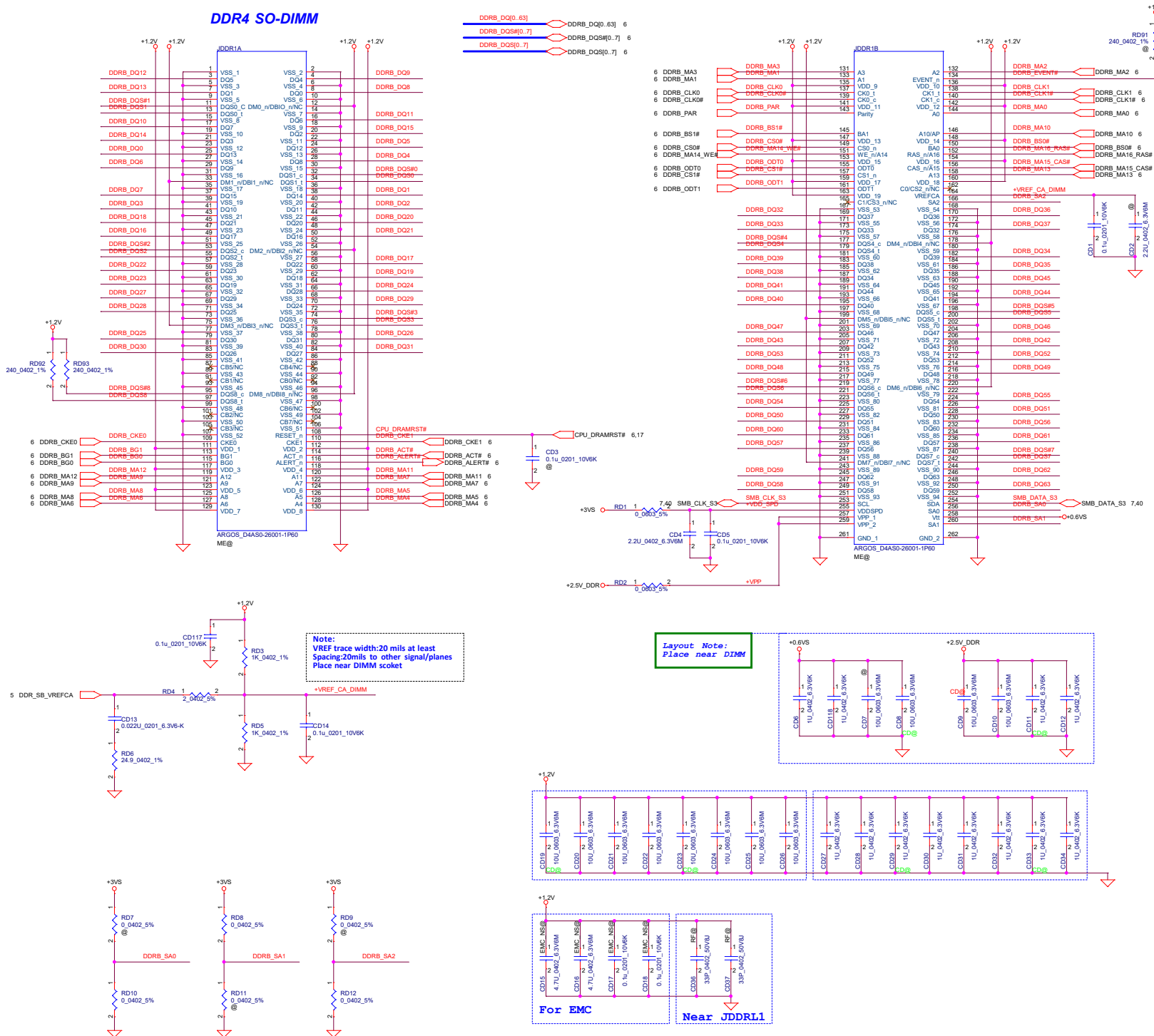


Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	- 1 = eDP Disabled - 0 = eDP Enabled★	1


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DDR4 SO-DIMM



SPD Address = 2H

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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

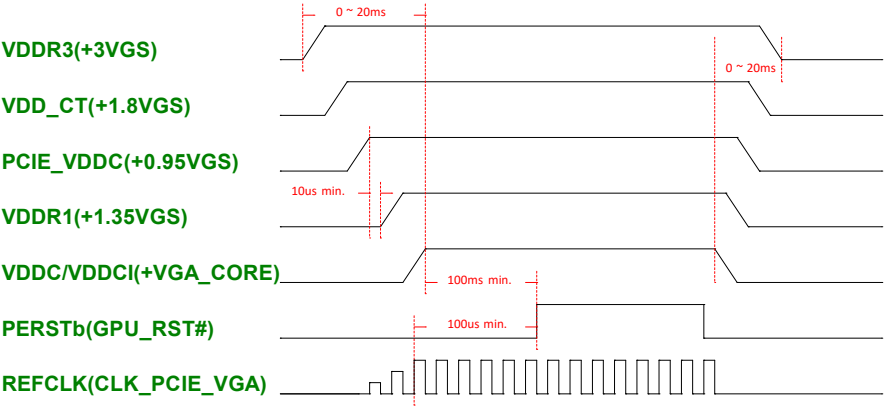
It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

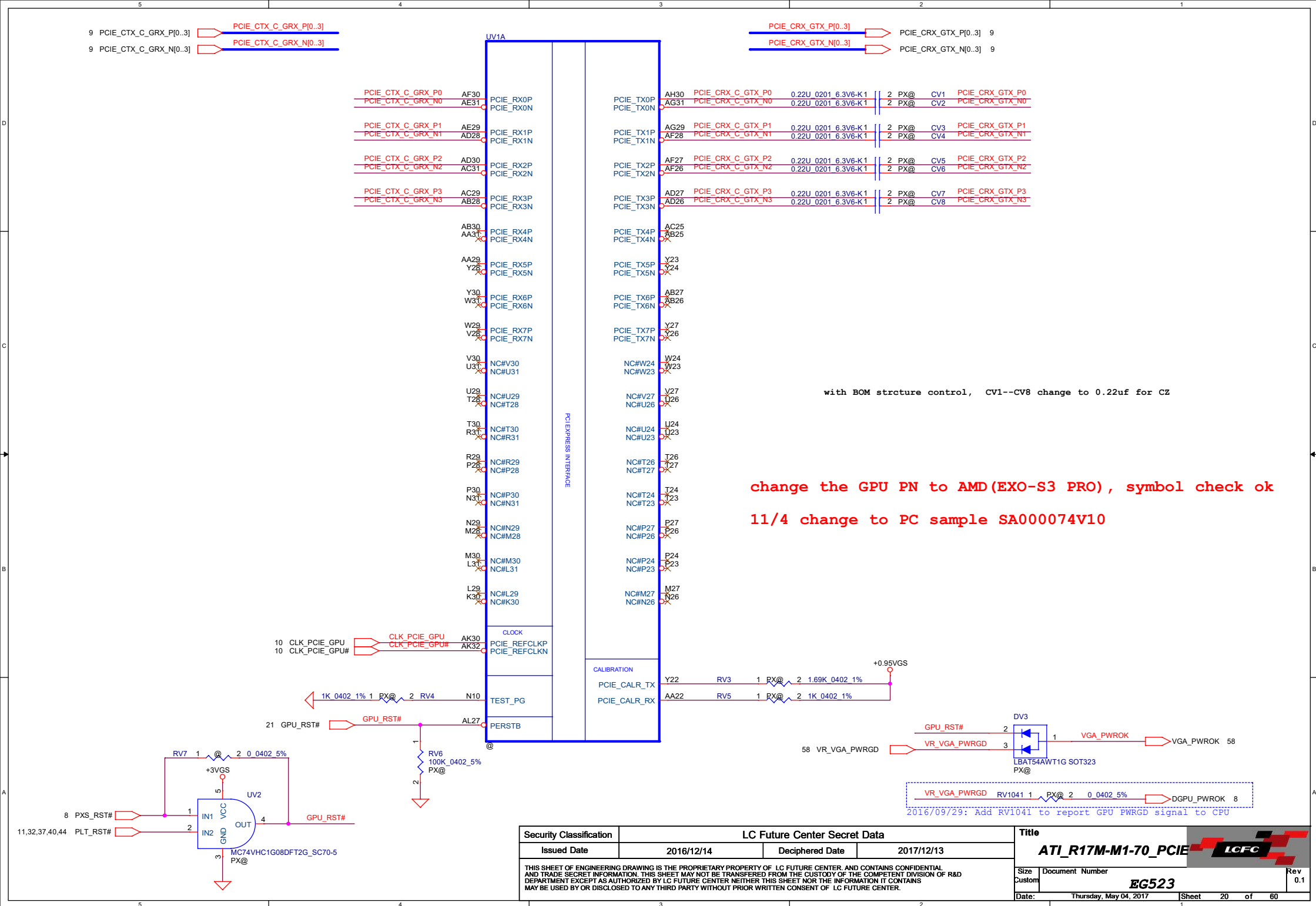
The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s)

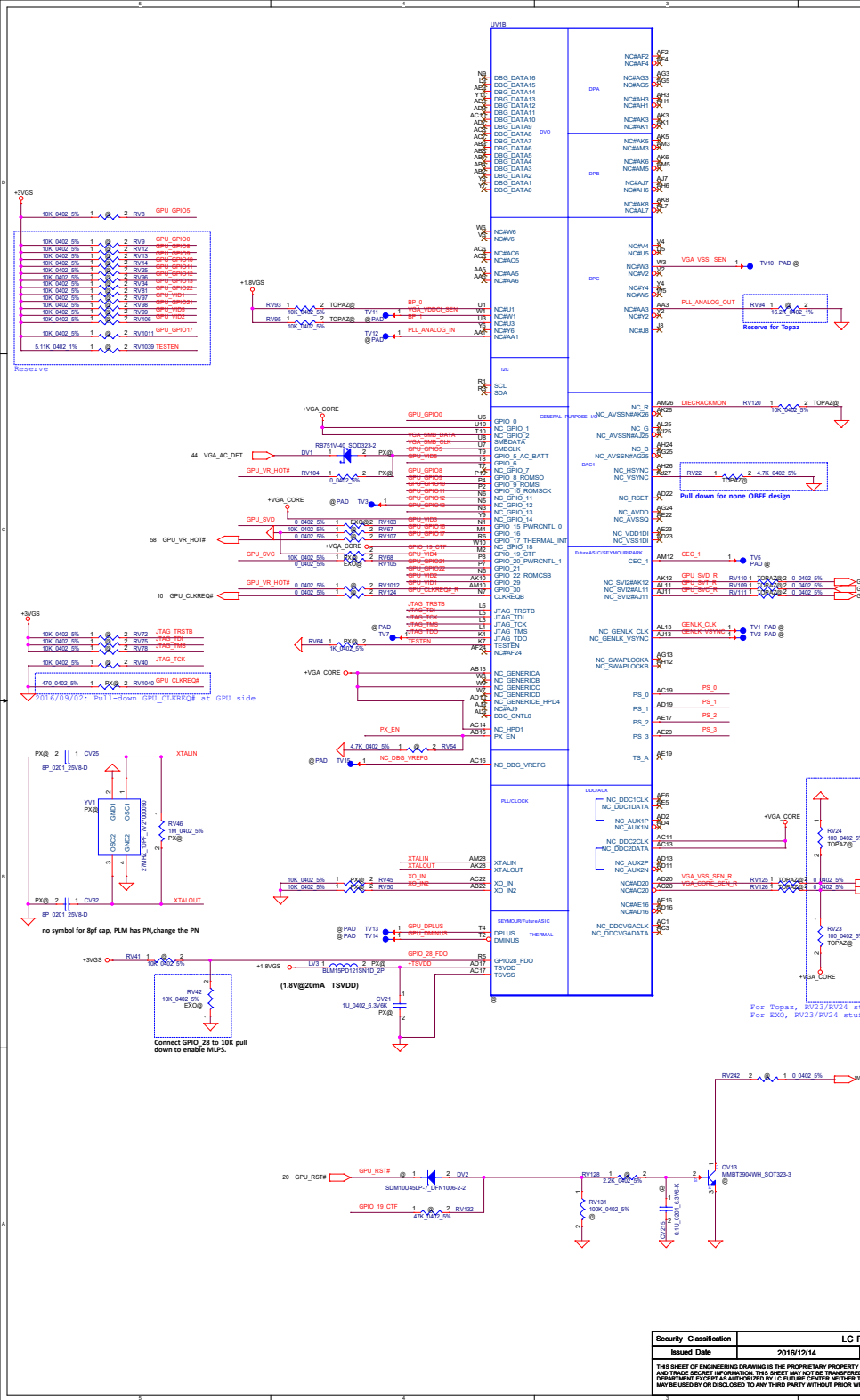
For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
4Gb GDDR5 256M x 16	Hynix H5GC4H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron EDW4032BABG-70-F 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G41325FE-HC28 6.0Gbps@1.35V	110	3.4K	10K
8Gb GDDR5 512M x 16	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70-A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

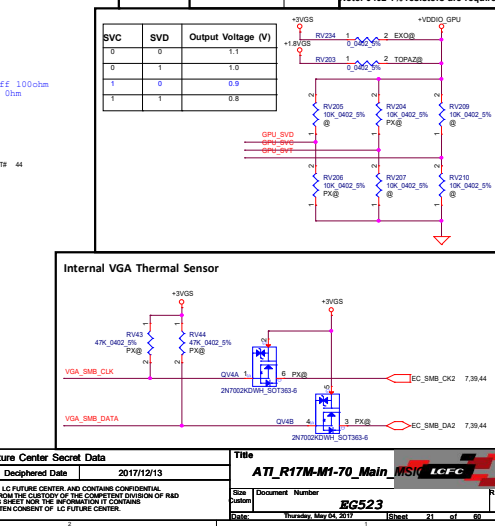
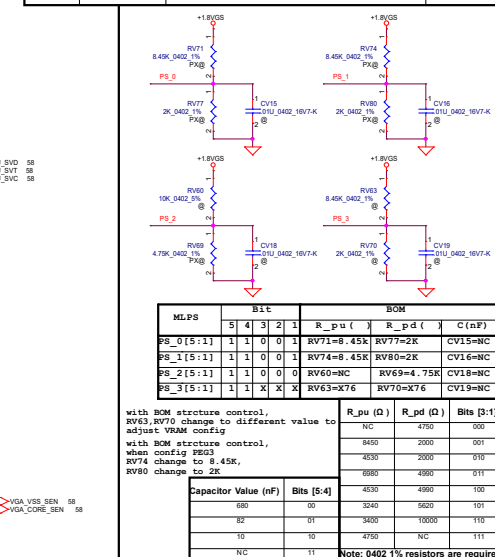




CONFIGURATION STRAPS

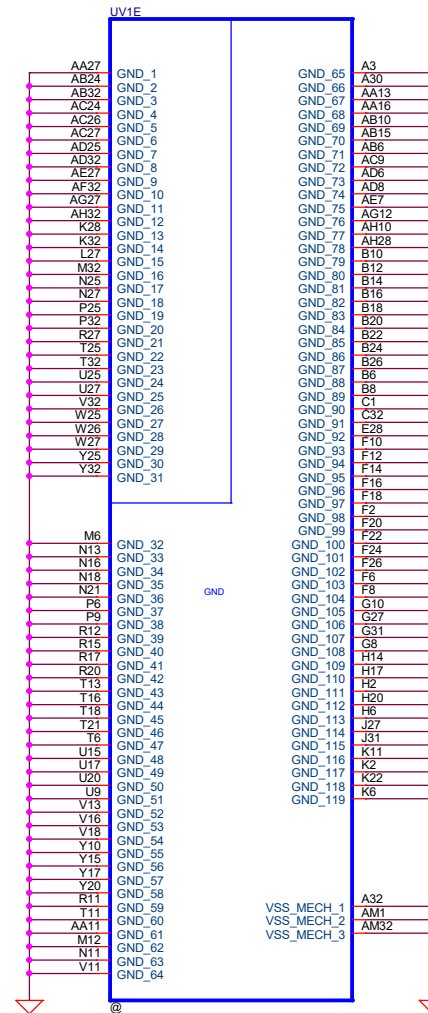
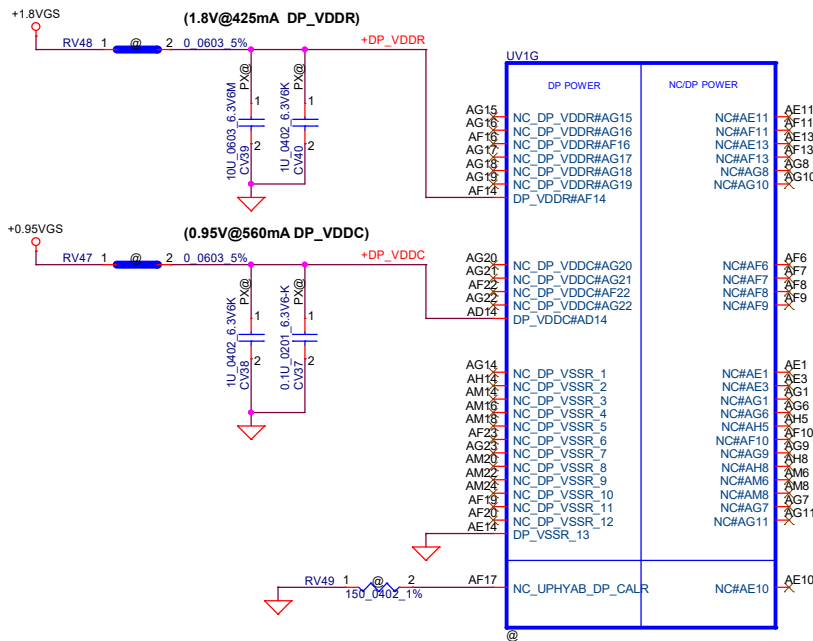
ALLOW FOR PULL-UP STRAPS FOR THESE STRAPS AND IF THESE
GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET


MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_0[0]	ROM_CONFIG[1]	Define the primary memory aperture size when STRAP_BIOS_ROM_EN = 0	001 = 256MB
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is supported. 1 = PCIe GEN3 is not supported.	1 = GEN3 is supported
PS_1[12]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled. 1 = The CLKREQ power management capability is enabled.	0
PS_1[13]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[14]	STRAP_TX_DRV_FULL_SWING	0 = The transmitter full-swing is enabled. 1 = The transmitter full-swing is disabled.	1
PS_1[15]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	1 = Enable
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capable enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved.	1
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap, such as for memory ID	
PS_3[2]	BOARD_CONFIG[1]	100 = Hynix 4Gb 101 = Hynix 8Gb 110 = Samsung 4Gb 000 = Hynix 8Gb 010 = Hynix 8Gb 001 = Samsung 8Gb	x
PS_3[3]	BOARD_CONFIG[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and used (Combine with PS_0[5])	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]		

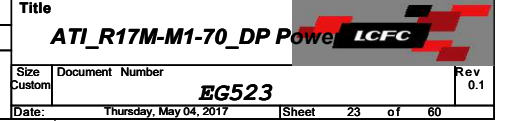


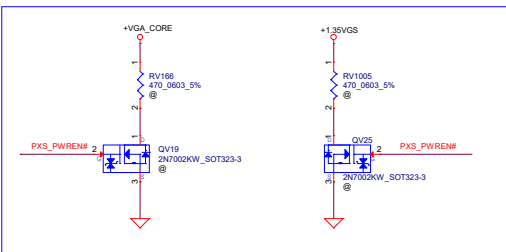
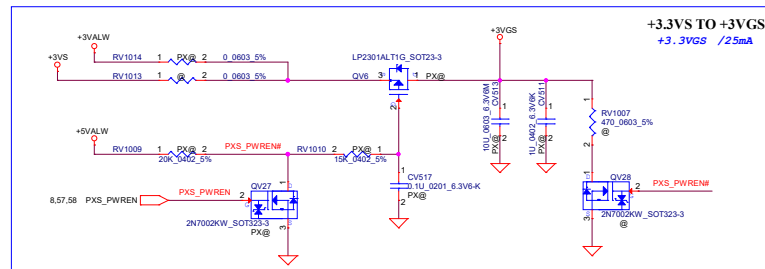
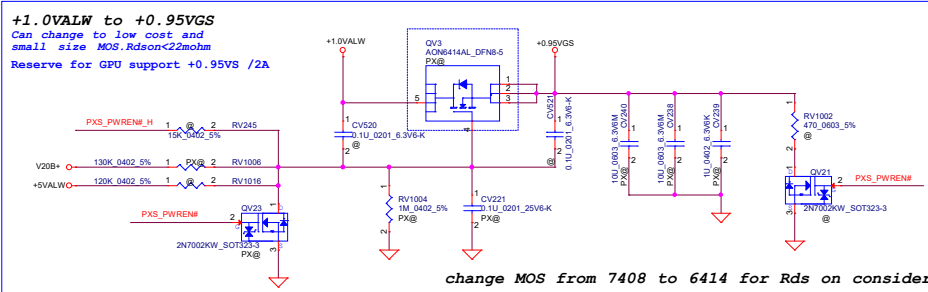
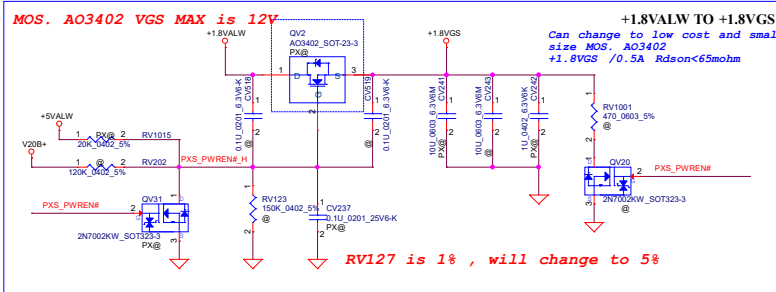
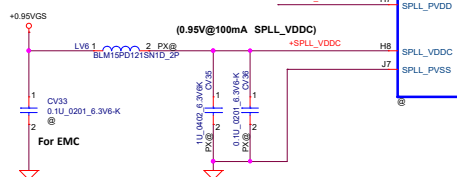
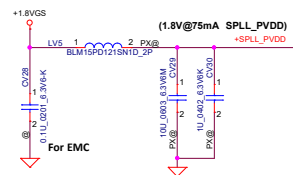


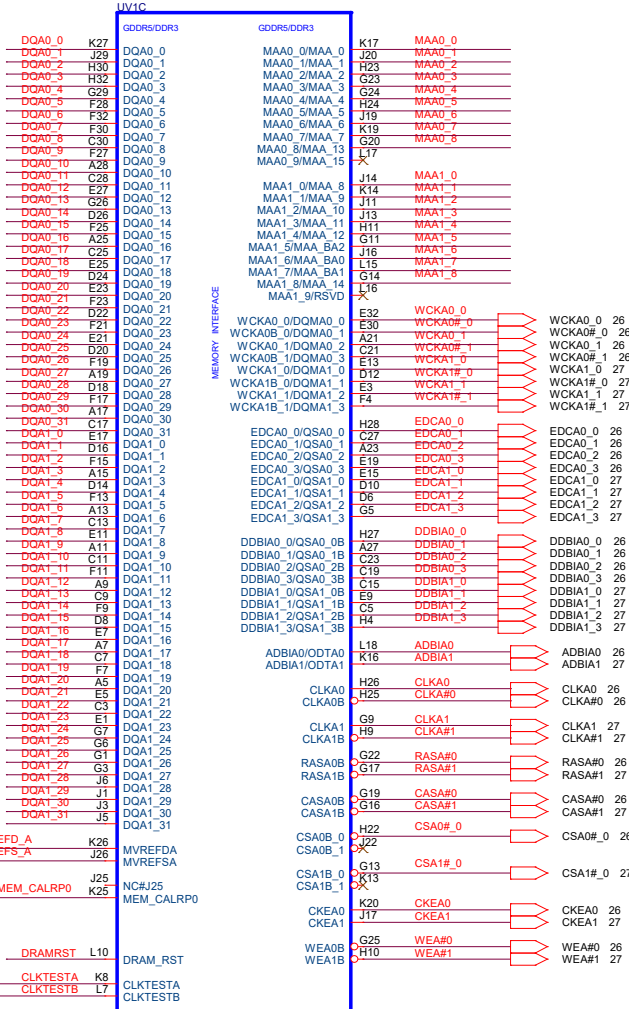
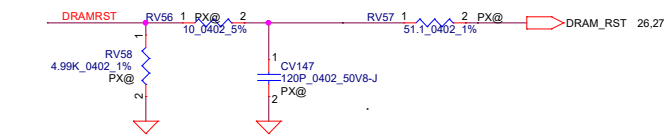
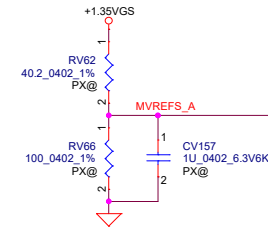
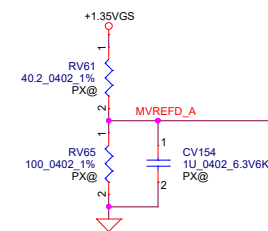
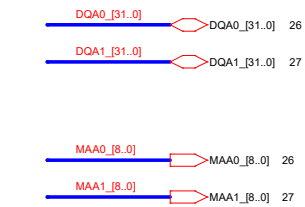
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2016/12/14	Deciphered Date	2017/12/13	ATI_R17M-M1-70_TMDP	
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				Date: Thursday, May 04, 2017	Rev 0.1
				Sheet 22	of 60




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Issued Date		2016/12/14		Deciphered Date		2017/12/13		ATI_R17M-M1-70_DP Power			
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</p>											
Size Custom						Document Number				Rev 0.1	
						EG523					
Date:						Thursday, May 04, 2017				Sheet 23 of 60	







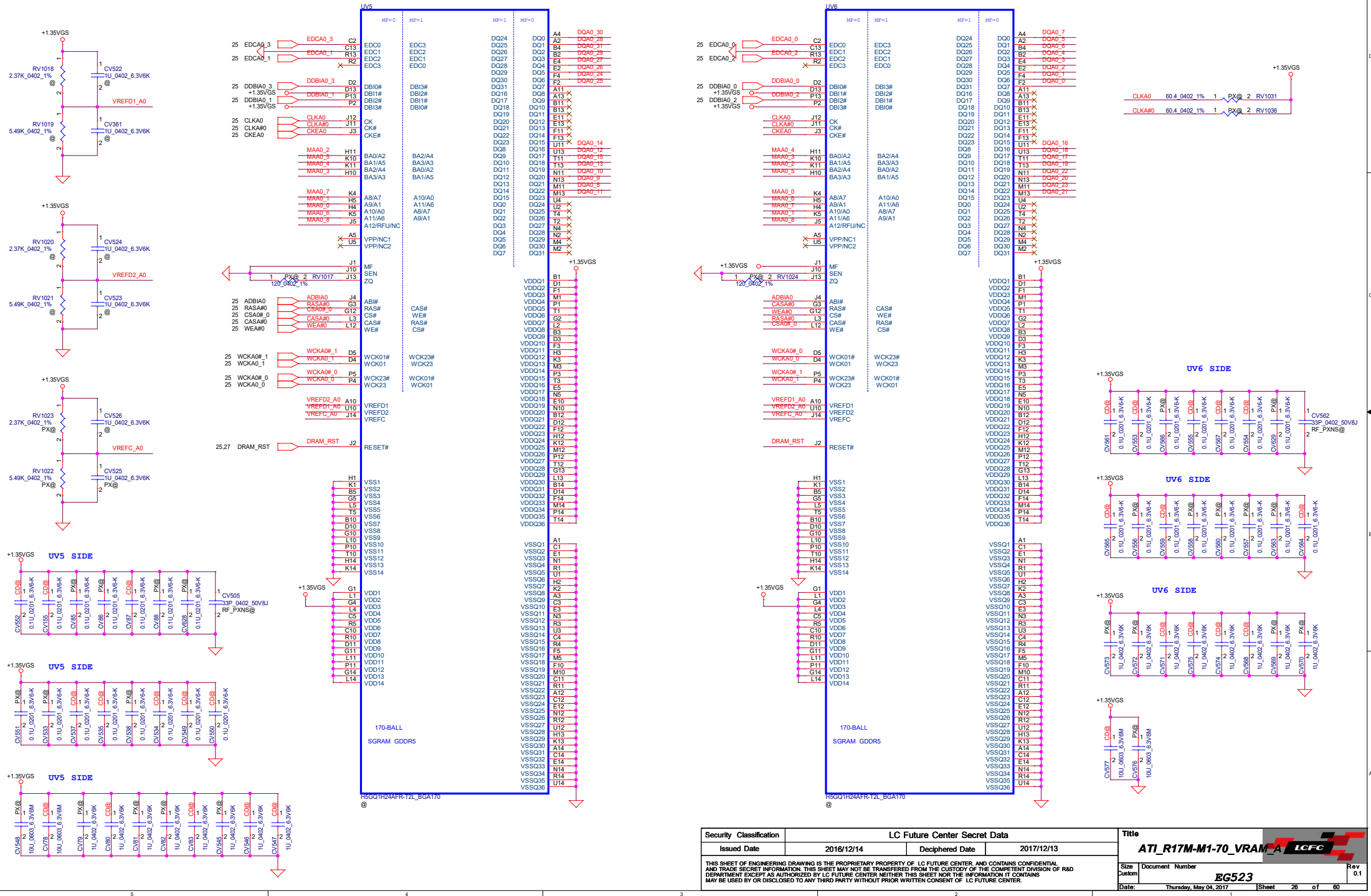
Security Classification		LC Future Center Secret Data				Title					
Issued Date		2016/12/14		Deciphered Date		2017/12/13					
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						Size		Document Number		Rev	
						Custom		EG523		0.1	
						Date:		Thursday, May 04, 2017		Sheet 25 of 60	
						3		1		2	

Lower 32 bits



MF=0 No Mirror

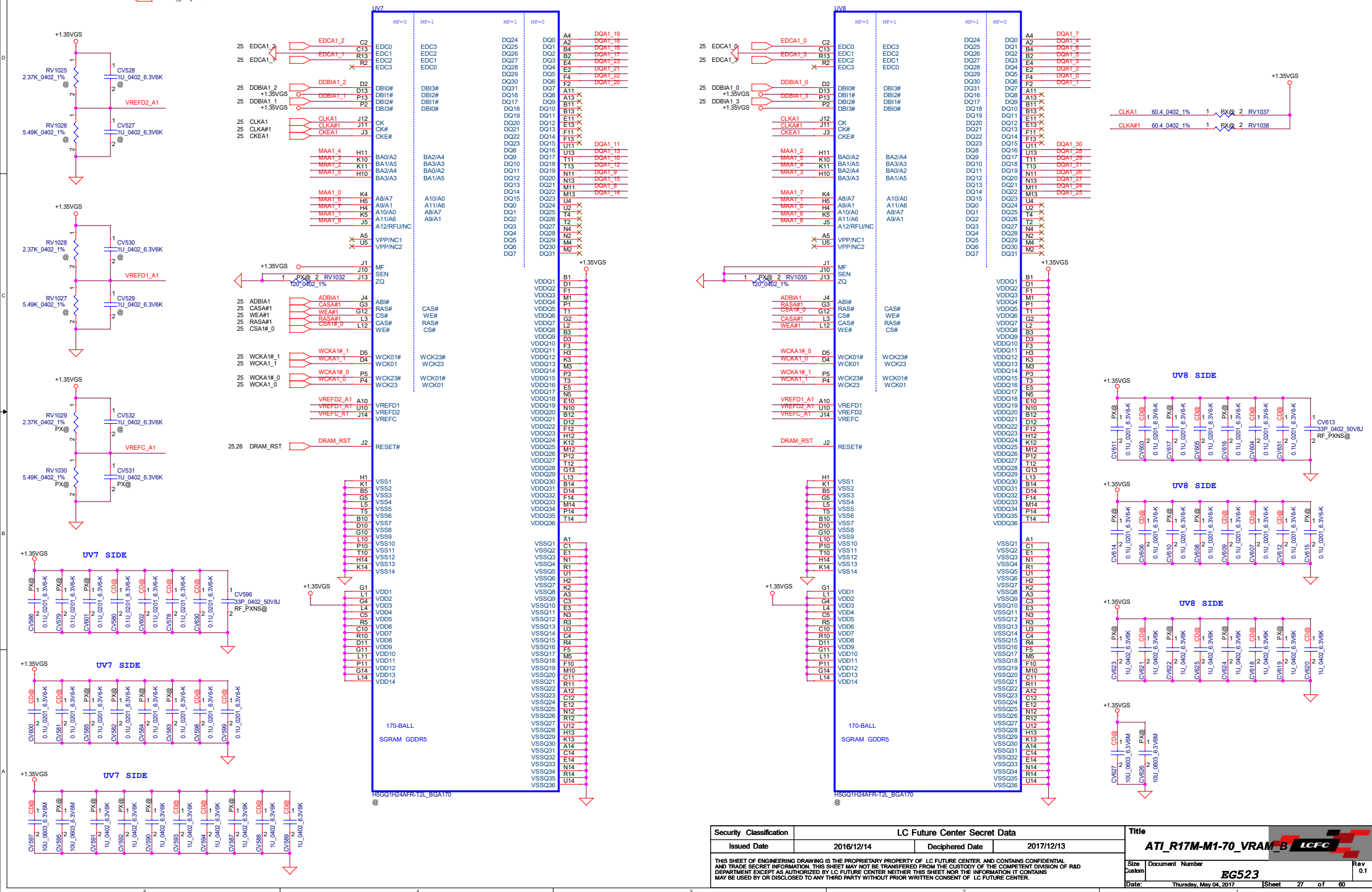
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		ATI_R17M-M1-70_VRAM_A	
2016/12/14		2017/12/13		LCFC	
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Date:		Thursday, May 04, 2017		Sheet 26 of 60	


 DQA1_[31..0] 25
 MAA1_[8..0] 25

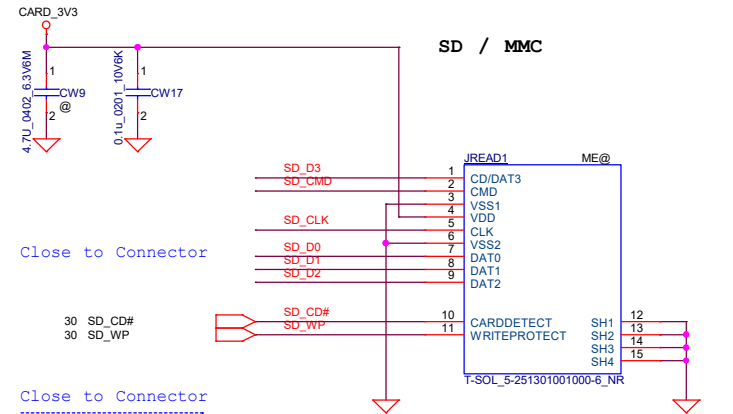
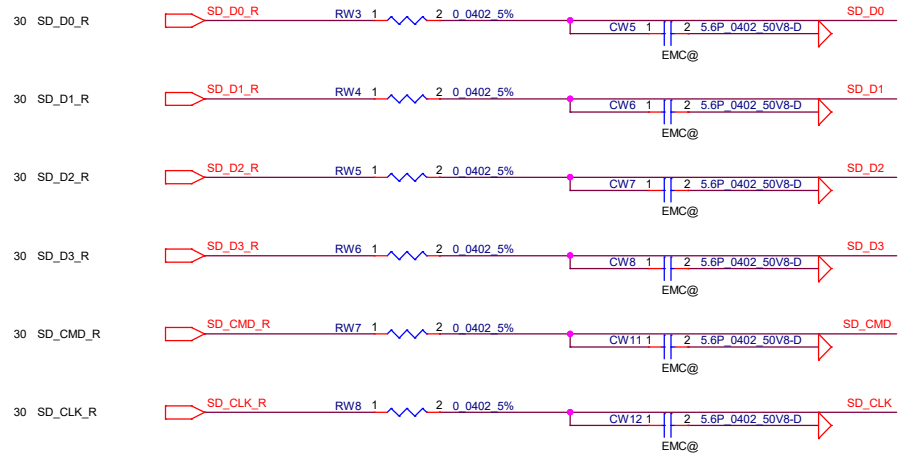
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Security Classification	LC Future Center Secret Data			Title	ATI_R17M-M1-70_VRAM_B 		
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Size	Document Number	EG523	
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				Date:	Thursday, May 04, 2017	Sheet	27 of 60

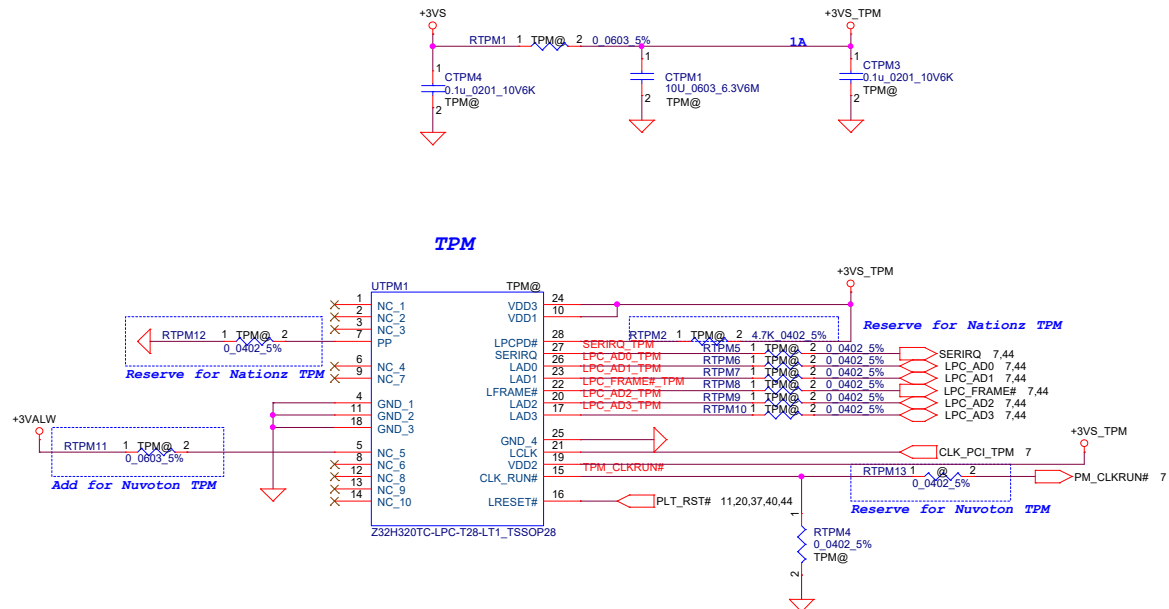
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D																								
C																								
B																								
A																								
Security Classification					LC Future Center Secret Data															Title				
Issued Date					2016/12/14					Deciphered Date					2017/12/13					Blank				
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																				Date: Thursday, May 04, 2017				
																				Sheet 28 of 60				

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Issued Date	2016/12/14	Deciphered Date	2017/12/13		
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				Date: Thursday, May 04, 2017	Sheet 29 of 60
				Rev 0.1	




8/16 Update Conn. P/N SP07000WG00 wei

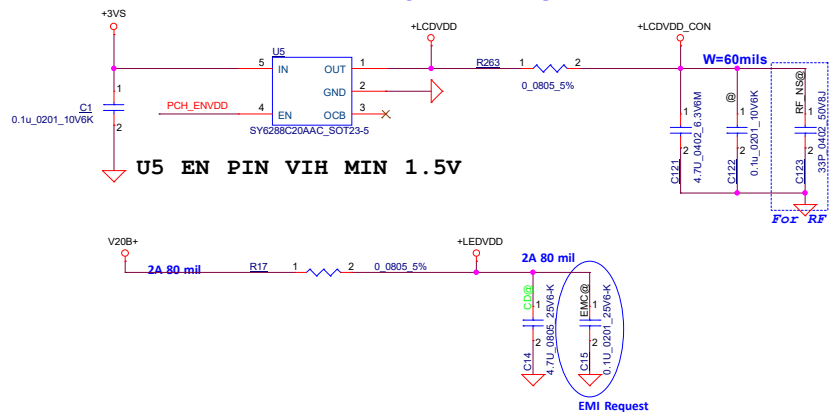
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Issued Date	2016/12/14	Deciphered Date	2017/12/13	Cardreader			
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				Date: Thursday, May 04, 2017	Sheet 31 of 60		



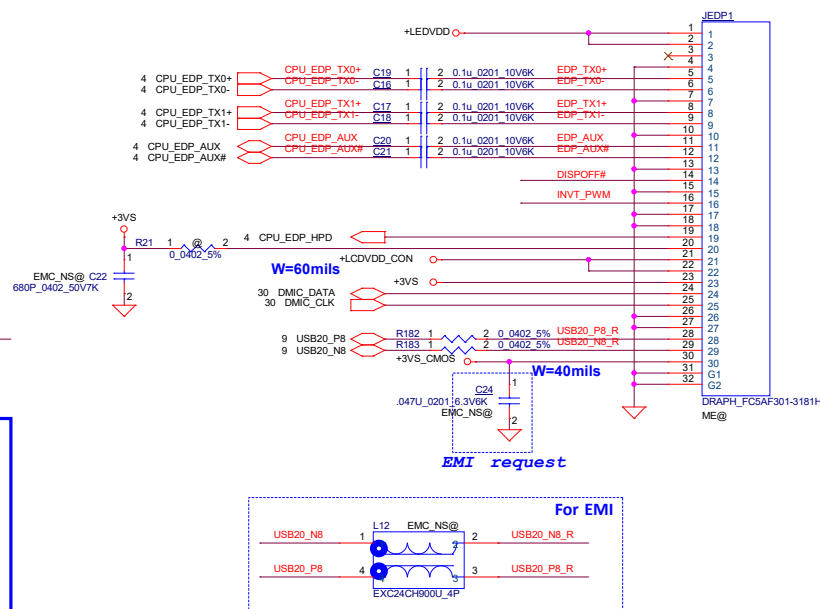
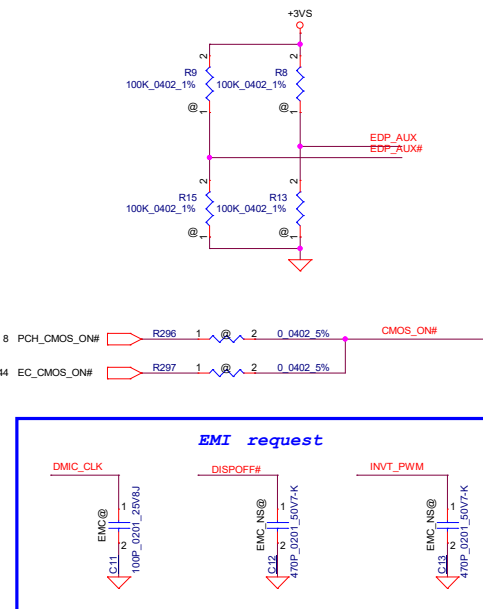
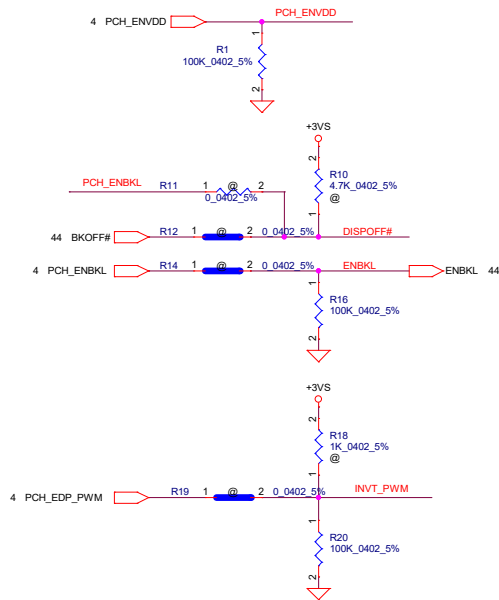
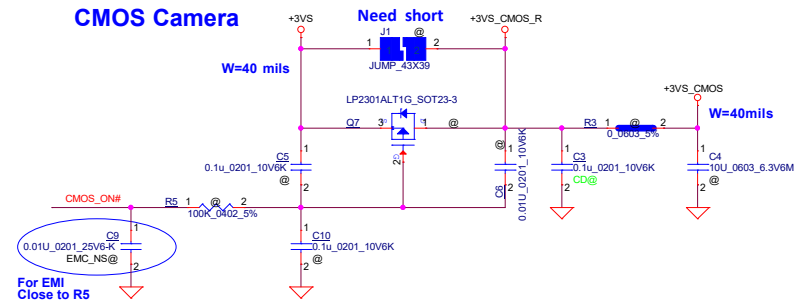
	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

Security Classification		LC Future Center Secret Data				Title											
Issued Date		2016/12/14		Deciphered Date		2017/12/13				TPM							
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Date:		Thursday, May 04, 2017				Sheet		32 of 60									

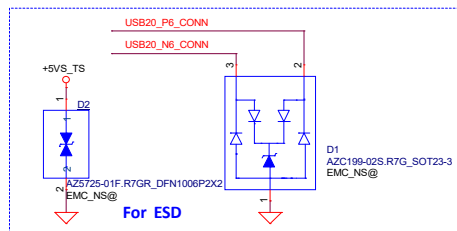
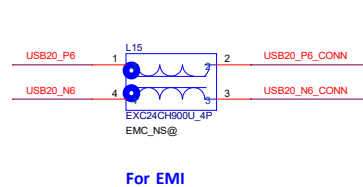
LCD POWER CIRCUIT



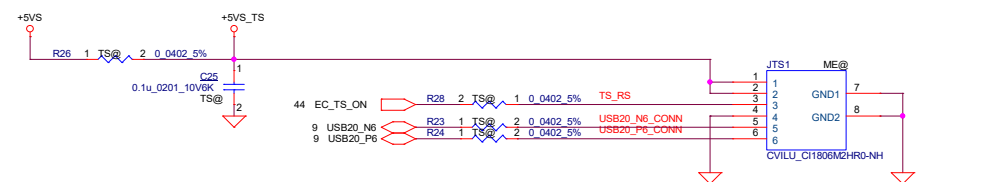
CMOS Camera



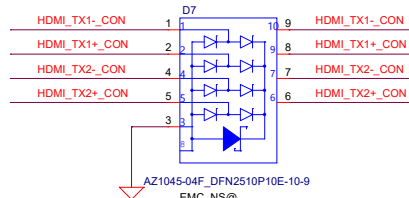
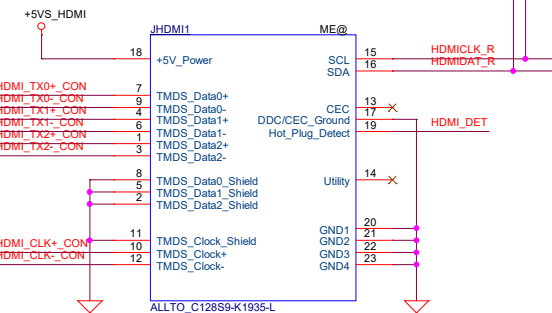
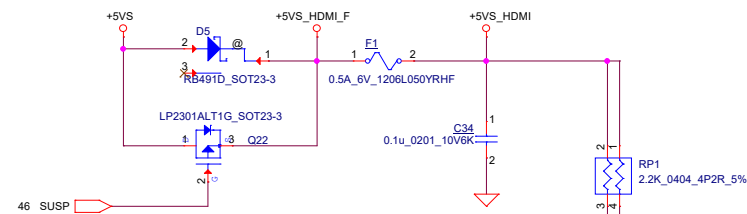
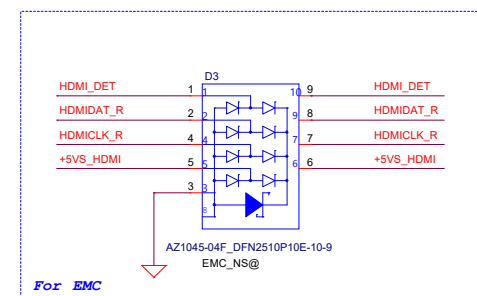
Touch Screen




Touch Screen

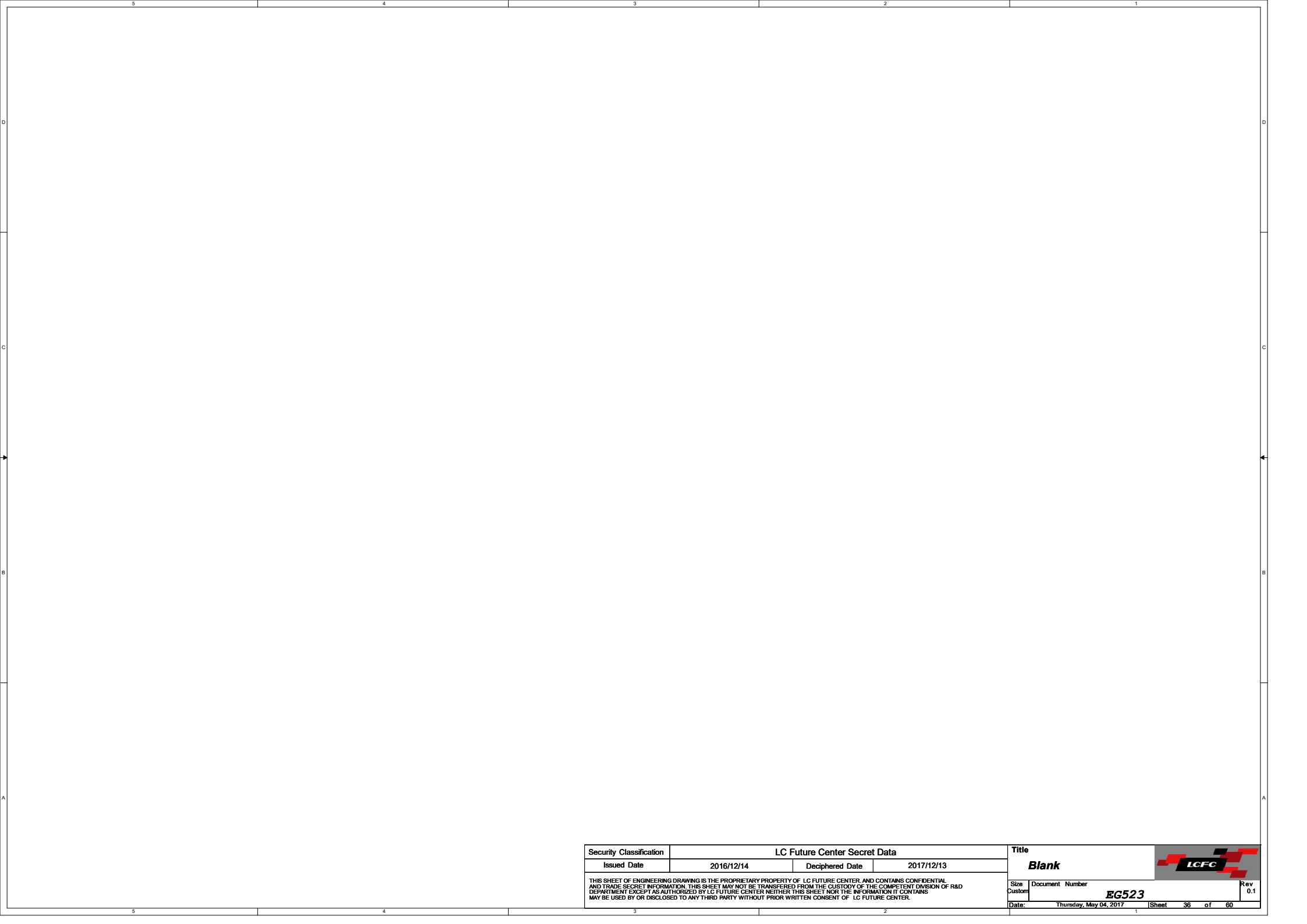



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Issued Date	2016/12/14	Deciphered Date	2017/12/13	eDP/CMOS/Touch screen	
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				Date:	Thursday, May 04, 2017
				Sheet	33 of 60

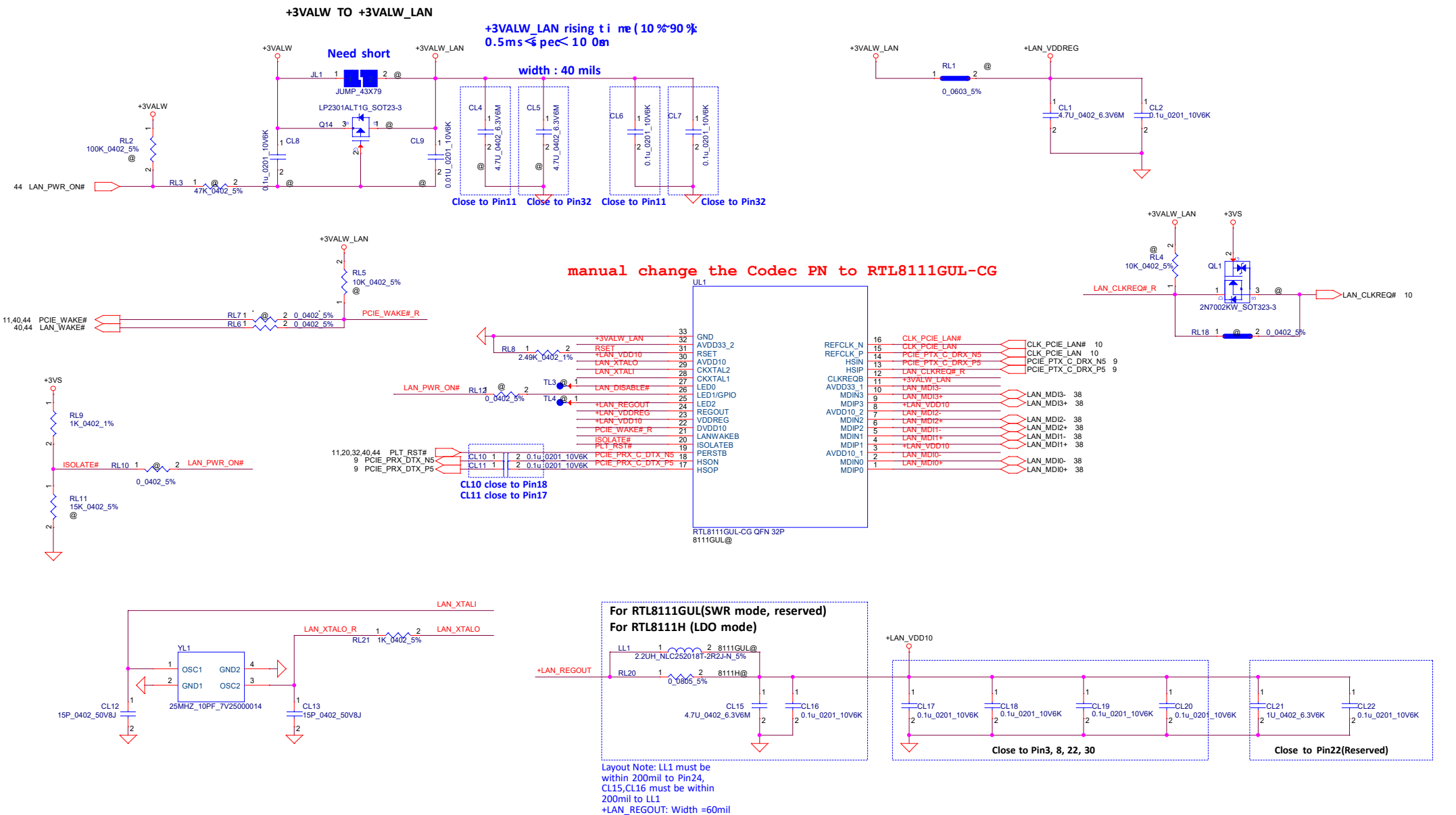



Size Custom	Document Number EG523	Rev 0.1
Date:	Thursday, May 04, 2017	Sheet 34 of 60

Security Classification				LC Future Center Secret Data				Title			
Issued Date		2016/12/14		Deciphered Date		2017/12/13		P35-Blank			
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Date: Thursday, May 04, 2017								Sheet 35 of 60			

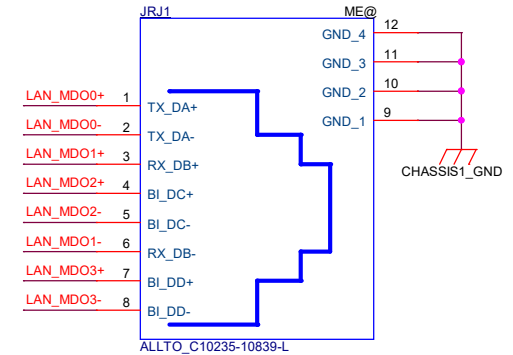
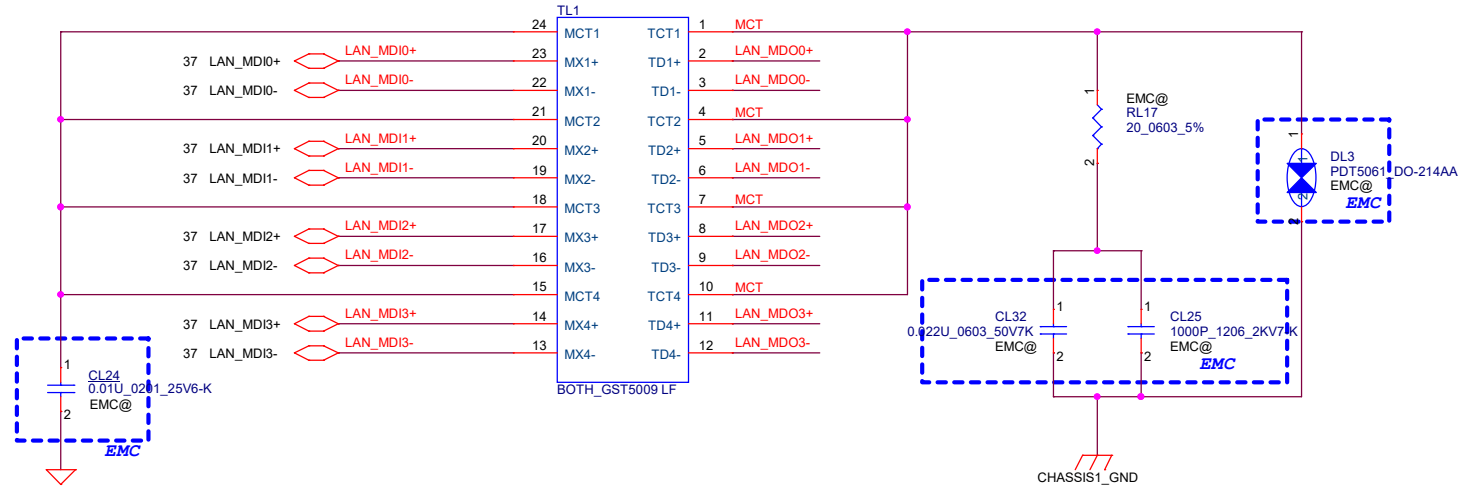
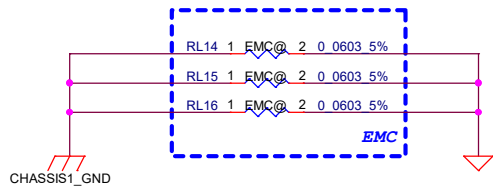
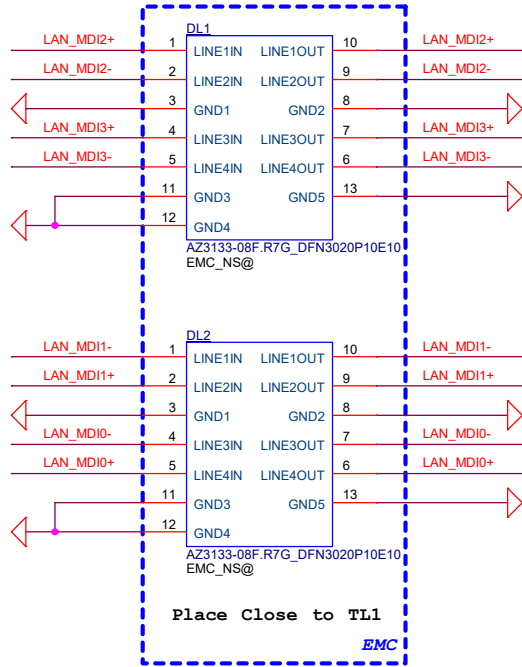


Security Classification		LC Future Center Secret Data		Title			
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				Custom	EG523	0.1	
Date:				Thursday, May 04, 2017 1 Sheet 36 of 60			




Security Classification		LC Future Center Secret Data			Title			
Issued Date		2016/12/14	Deciphered Date	2017/12/13	LAN_RTL8111H_CG			
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Size Custom		Document		Number		EG523		Rev 0.1
Date:		Thursday, May 04, 2017		Sheet		37 of 60		

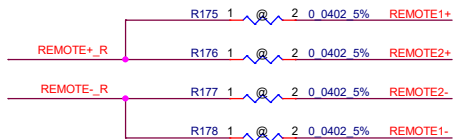
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8/16 Update RJ45 P/N DC021608091 wei

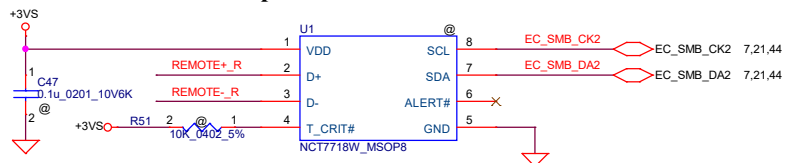
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2016/12/14	Deciphered Date	2017/12/13	LAN_Transformer			
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				3	EG523	0.1	
				Date:	Thursday, May 04, 2017	Sheet	38 of 60

Close to U1

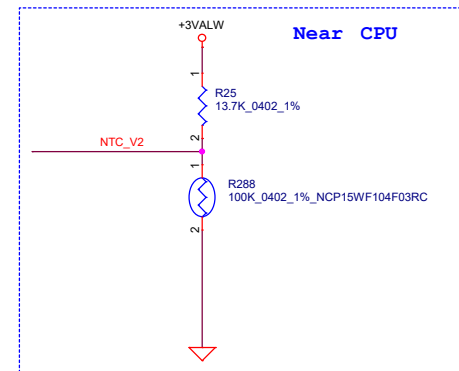
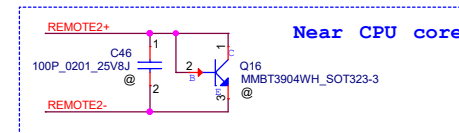
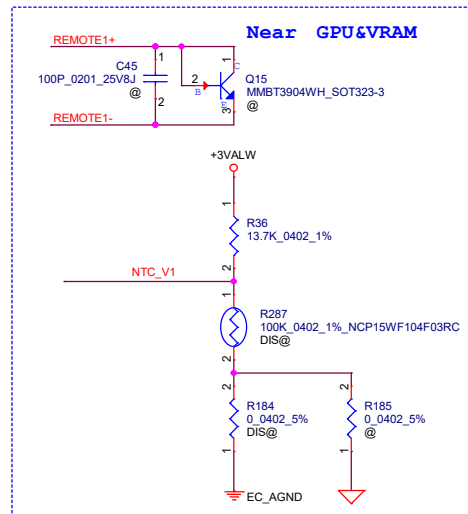


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

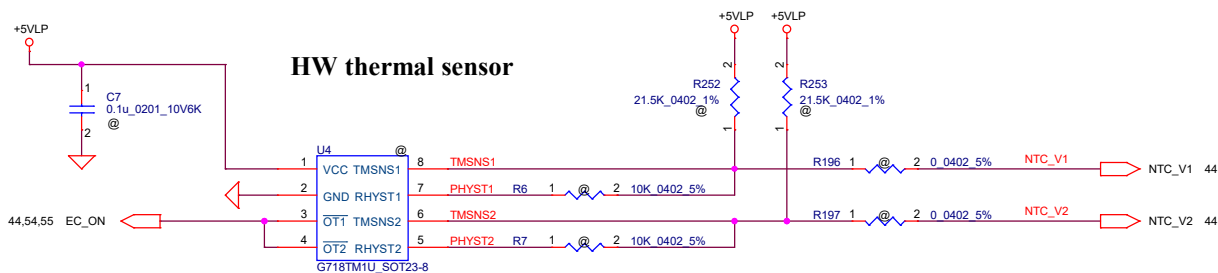
SMSC thermal sensor placed near DIMM



Address 1001_101xb

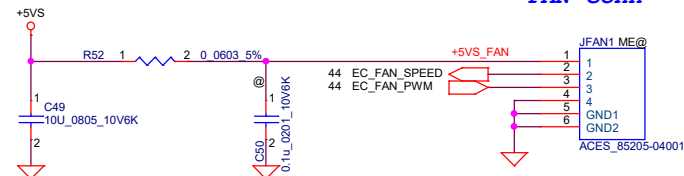


HW thermal sensor



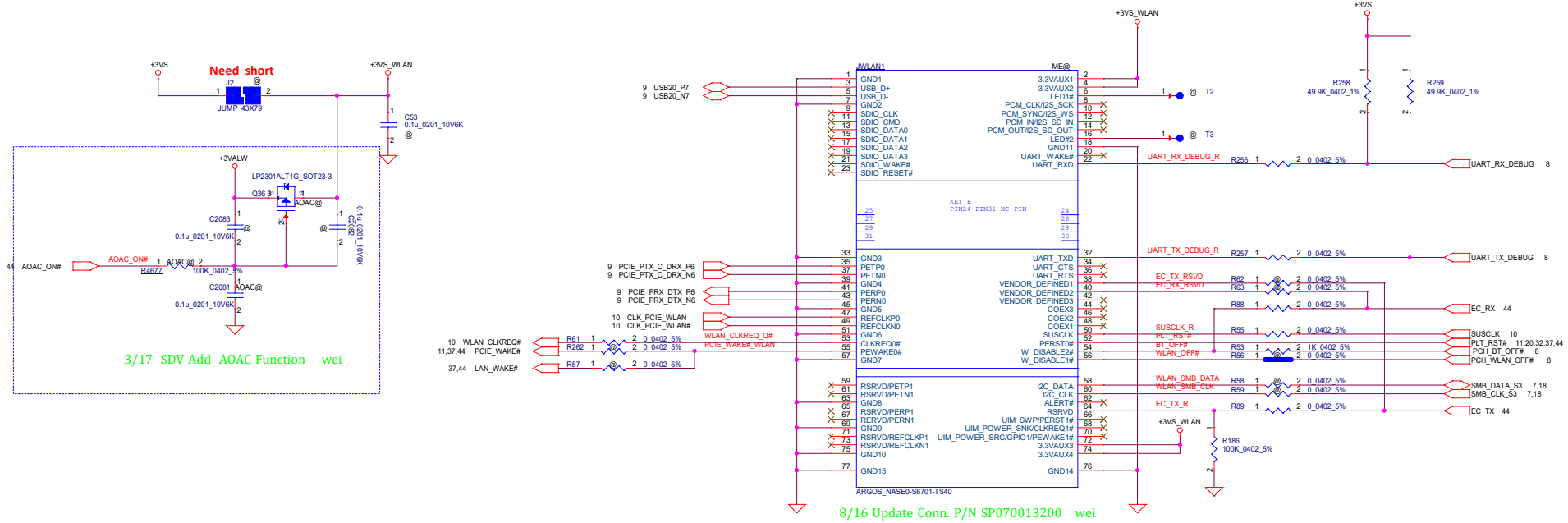
over temperature threshold:
 $RSET = 3 * RTMH$
92+/-30C
Hysteresis temperature threshold.
 $RHYST = (RSET * RTML) / (3 * RTML - RSET)$
56+/-30C

FAN Conn

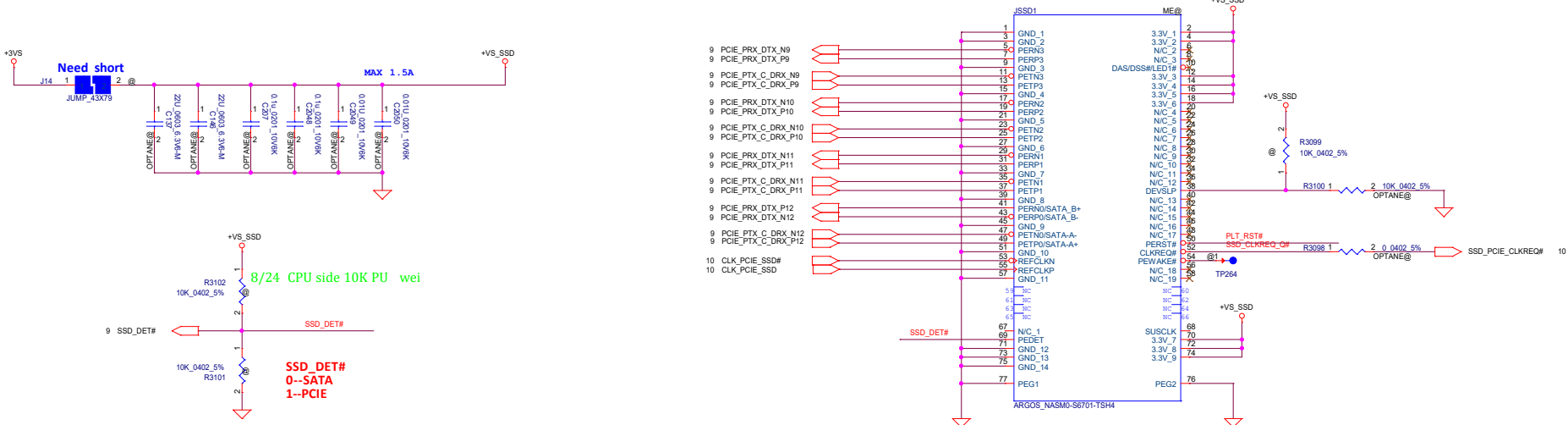


Security Classification	LC Future Center Secret Data			Title	Thermal sensor/FAN Conn	
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Size	Document Number	Rev
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				Date:	Thursday, May 04, 2017	Sheet 39 of 60

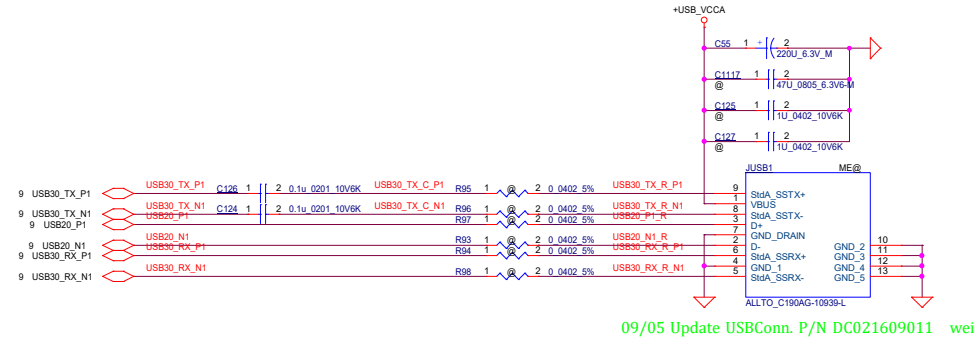
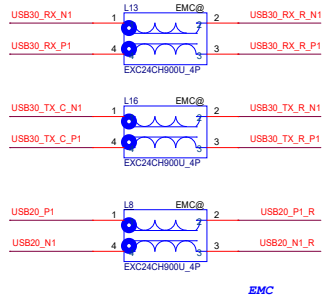
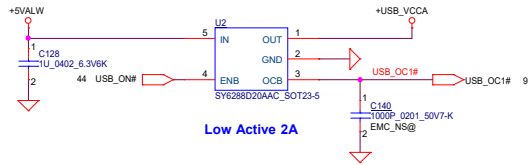
Mini-Express Card(WLAN/WiMAX)



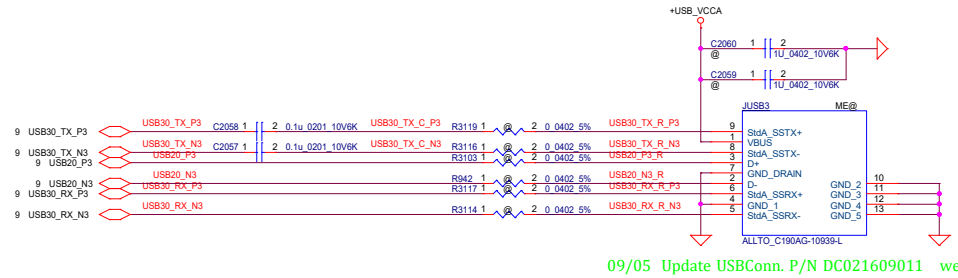
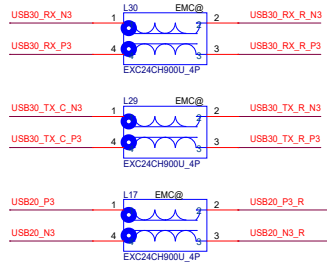
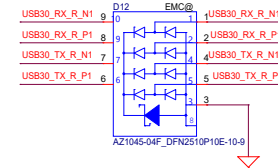
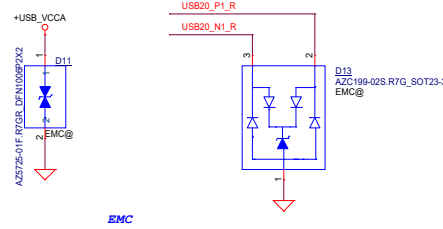
Optane Memory



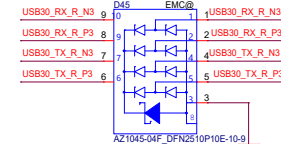
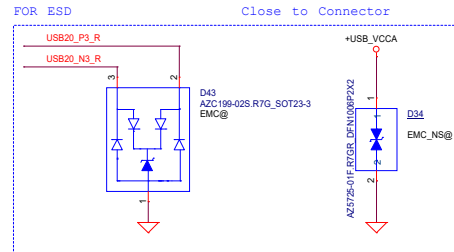
LEFT SIDE USB3.0 PORT x2



09/05 Update USBConn. P/N DC021609011 wei

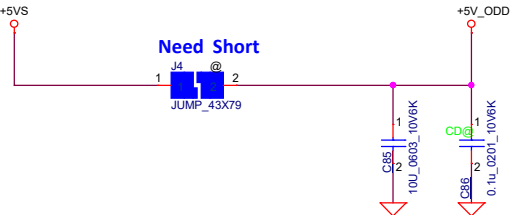
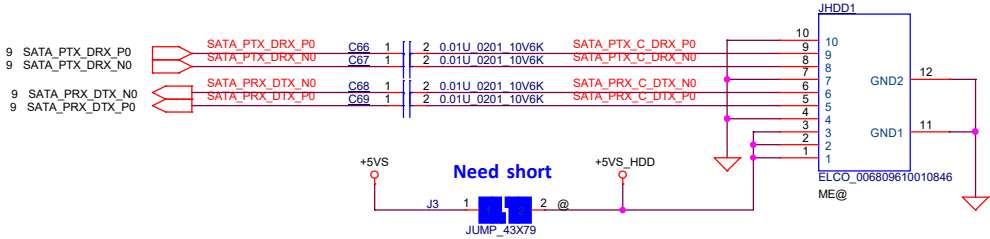
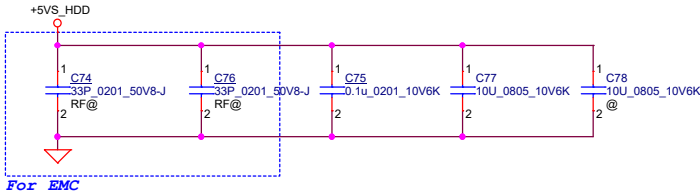


09/05 Update USBConn. P/N DC021609011 wei

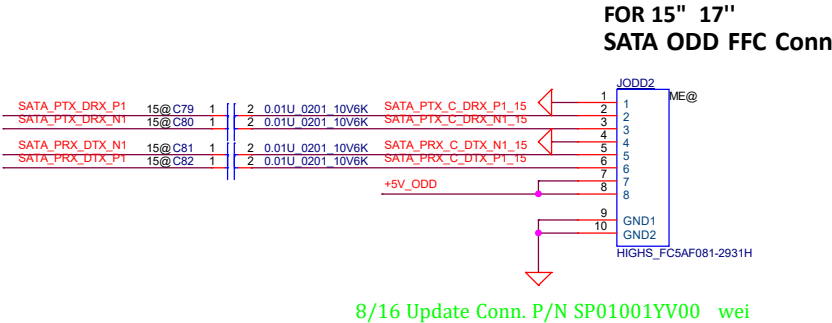


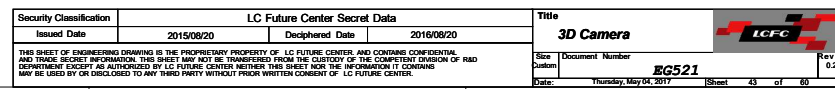
Security Classification	LC Future Center Secret Data		Title	USB3.0 PORT (LEFT)	
Issued Date	2016/12/14	Deciphered Date	2017/12/13	Size	Document Number
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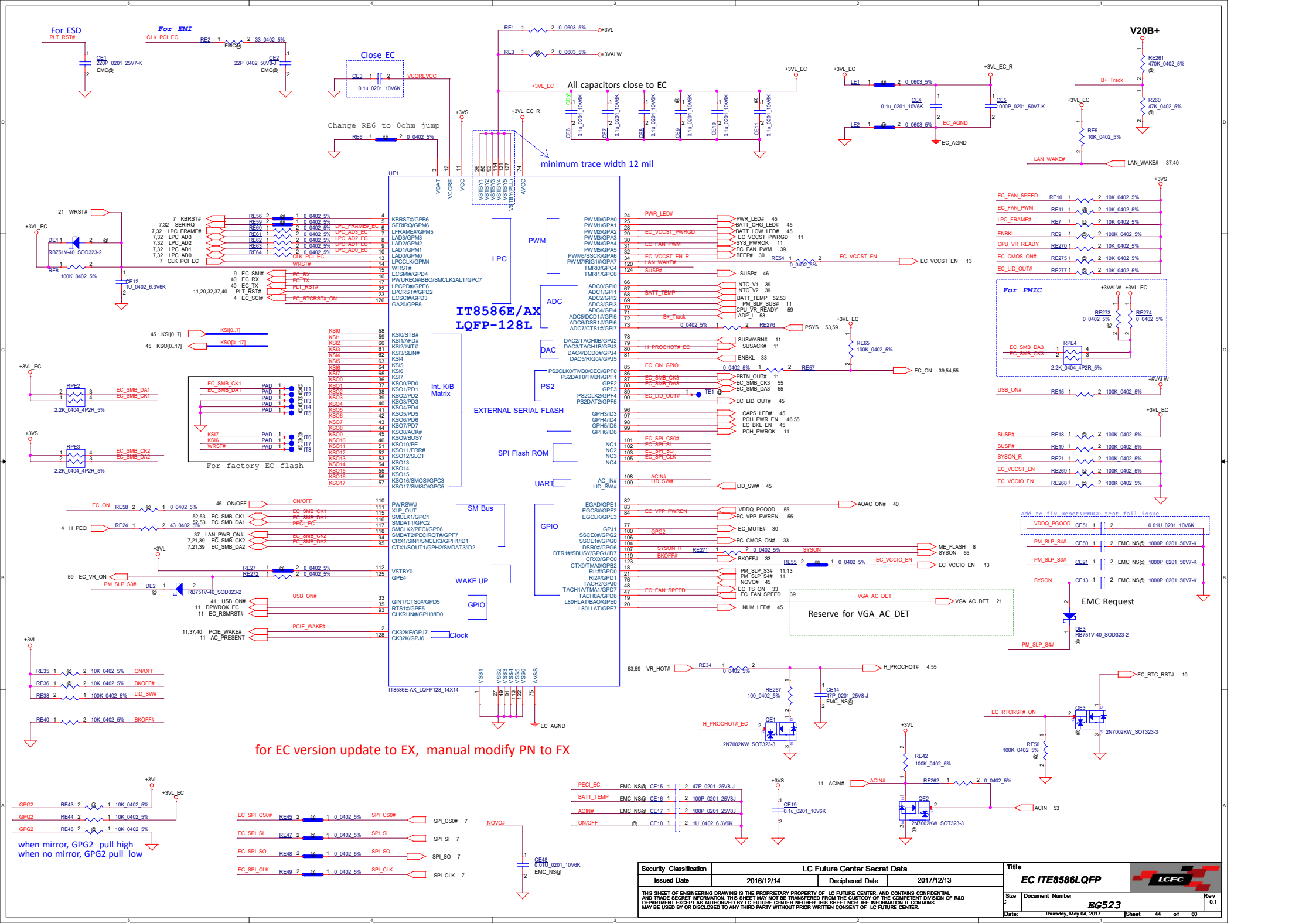
SATA HDD Conn.



FOR 14" SATA ODD Conn.



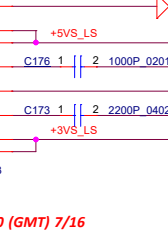
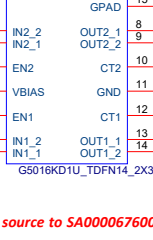
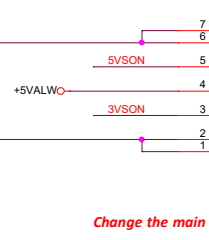
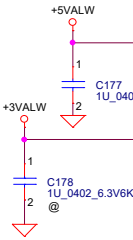
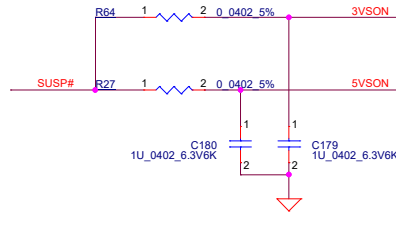




Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

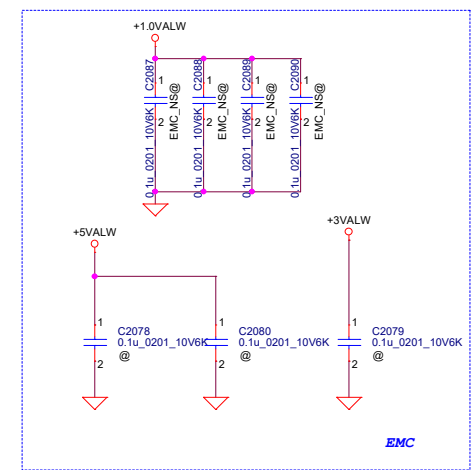
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



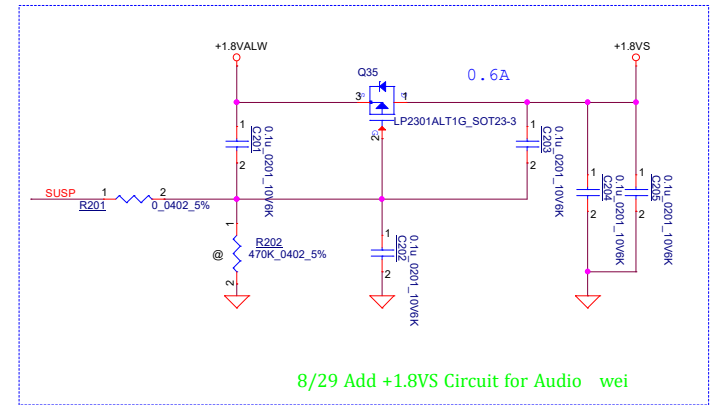
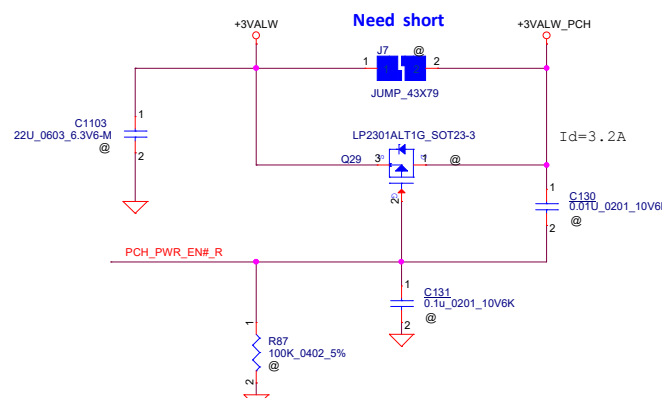
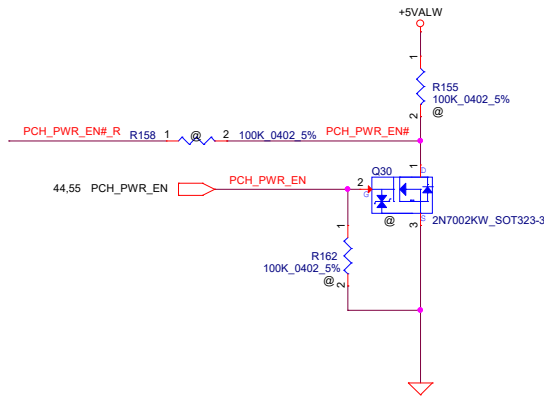
Need Short

Need Short

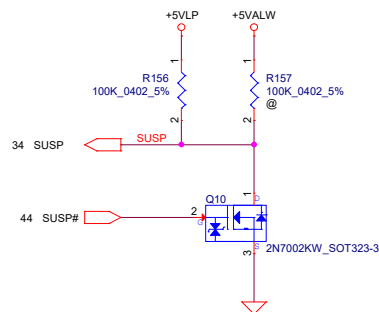
Change the main source to SA000067600 (GMT) 7/16



EMC



8/29 Add +1.8VS Circuit for Audio wei

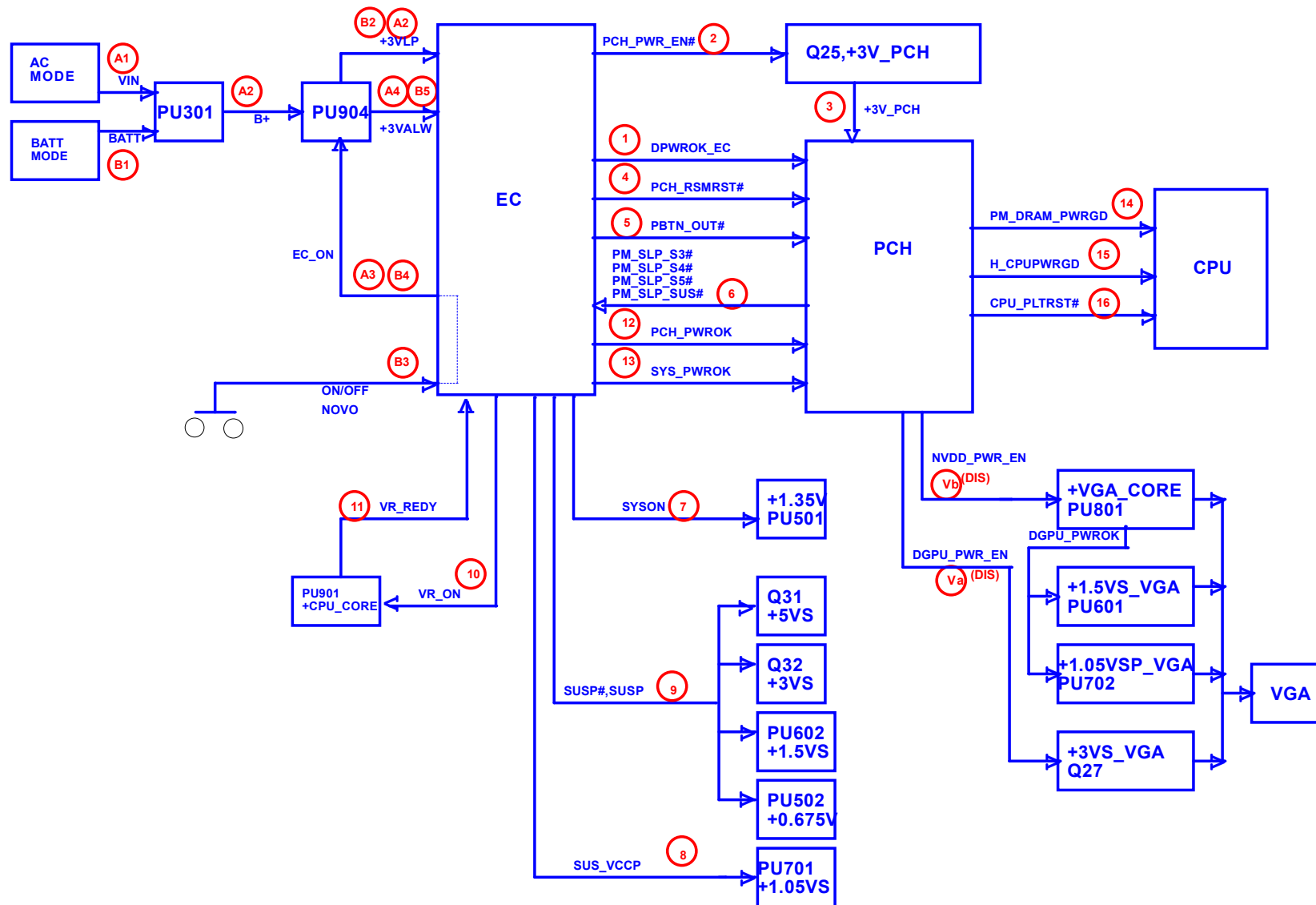


For DisCharge



08/29: Need double check enable signal and the resistance

Security Classification		LC Future Center Secret Data				Title		<div>DC V TO VS INTERFACE</div> <div>LCFC</div>	
Issued Date	2016/12/14	Deciphered Date	2017/12/13		Size	Document Number	Rev		
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Power sequence block		0.1	
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Custom			
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ZZZ1

NMB453@

NM-B453

DA600013Q00

HA

PCB_MB

UC1

I7@

KBL-R CPU

SA00008J600

UC1

I5@

KBL-R CPU

SA00008J500

CPU
CPU

UL1

8111H@

RTL8111H-CG

SA000074W00

LAN Chip

UL1

PX@

R17M-M1-70 GPU

SA000086K00

GPU

ZZZ2

DRAM_S4G@

Samsung

X7643712009

ZZZ2

DRAM_M4G@

Micron

X7643712008

ZZZ2

DRAM_H4G@

Hynix

X7643712007

2400MT/s DRAM X76 BOM

ZZZ4

S4GX4@

Samsung

X7643912002

ZZZ4

H4GX4@

Hynix

X7643912001

ZZZ4

M4GX4@

Micron

X7643912003

ZZZ4

S8GX4@

Samsung

X7643A12002

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Micron

X7643A12003

VRAM X76 BOM

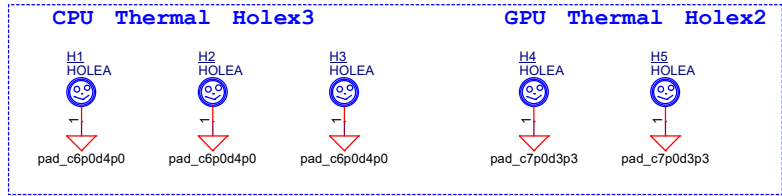
ZZZ3

HDMI@

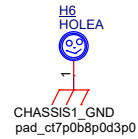
HDMI PN

RO00000040J

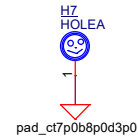
HDMI Royalty



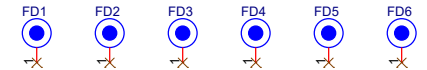
Close to RJ45



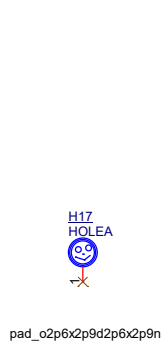
Close to Audio jack



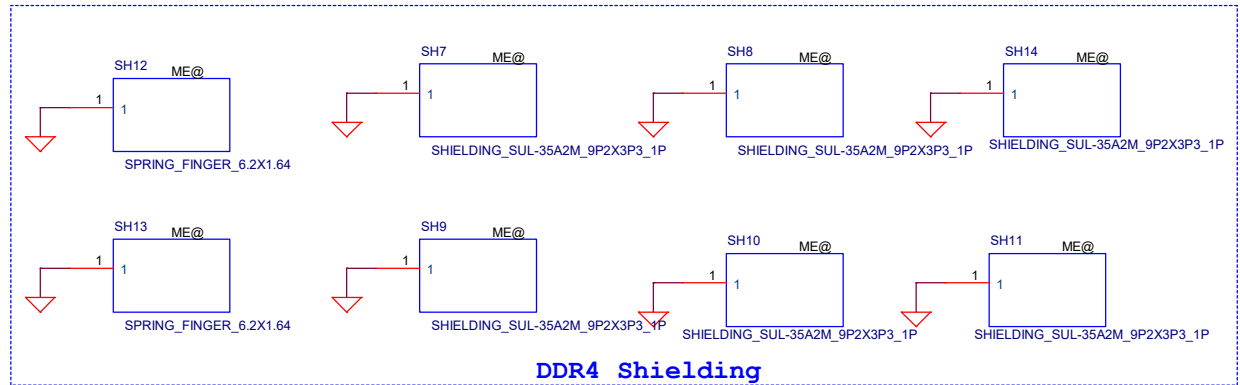
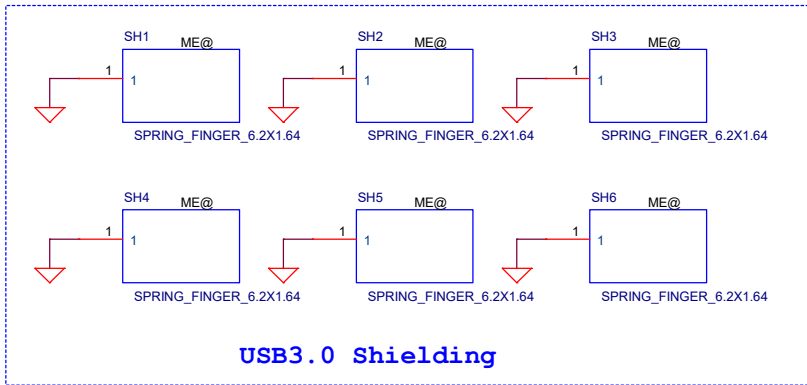
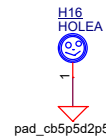
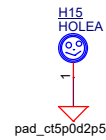
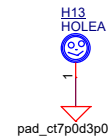
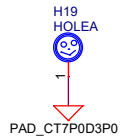
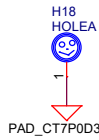
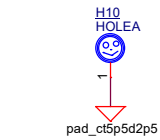
PCB Federal Mark PAD




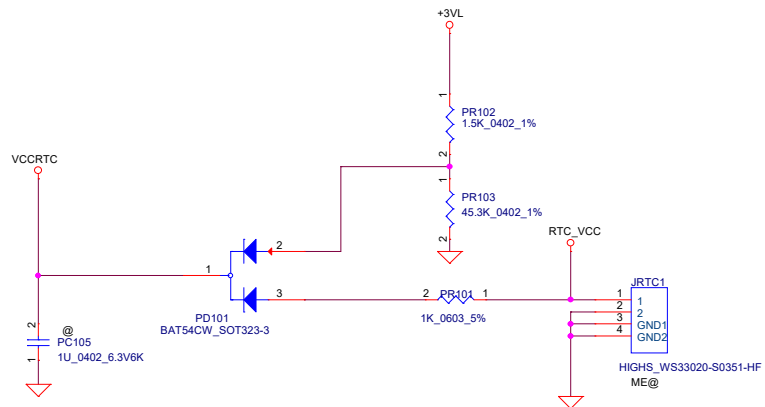
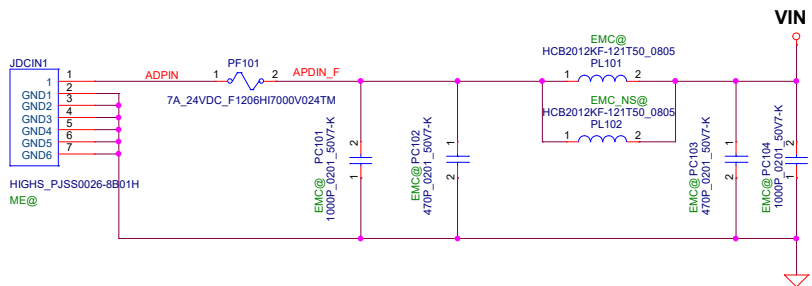
DC-IN x2



WLAN Standoff

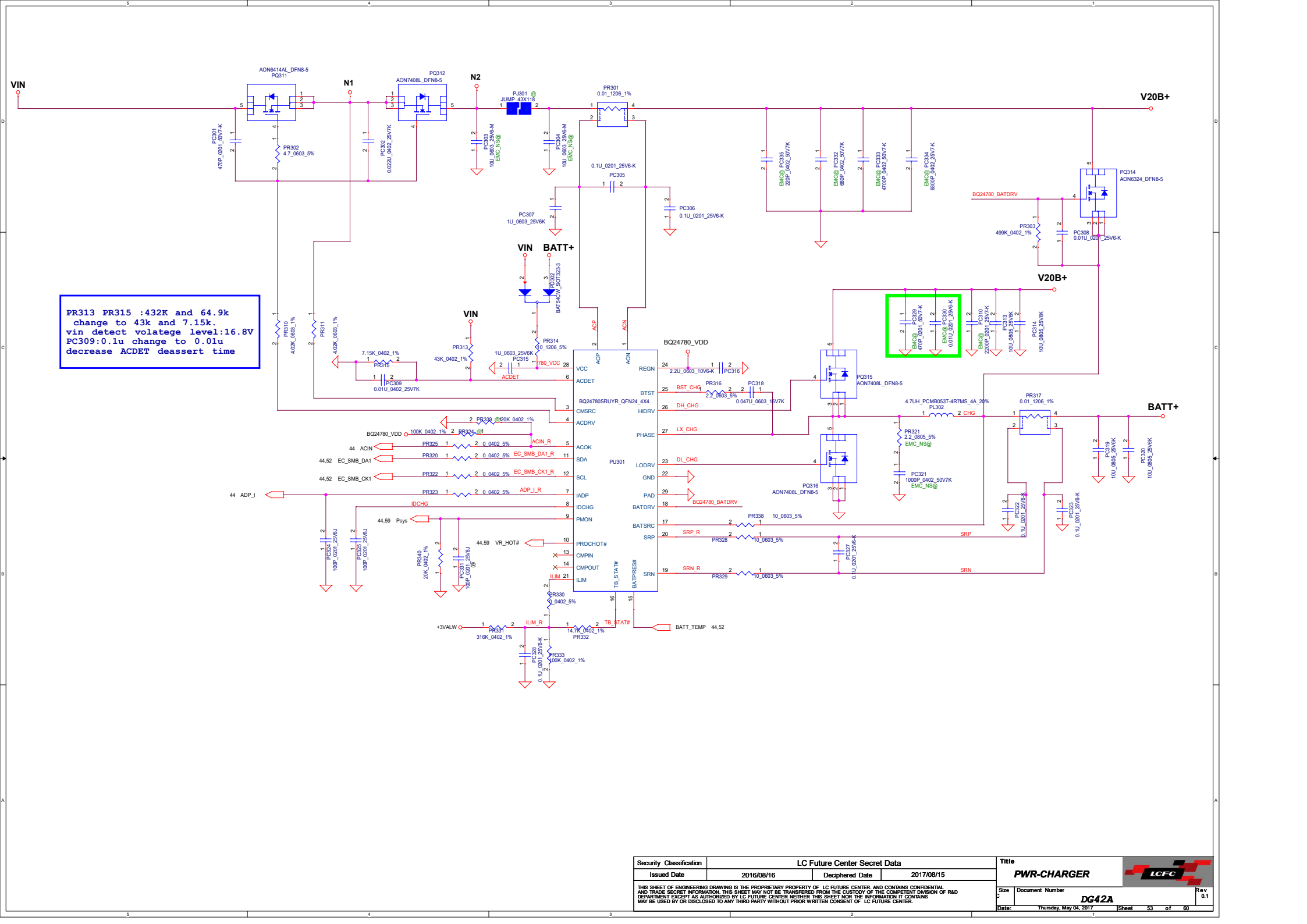


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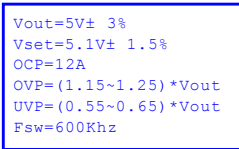
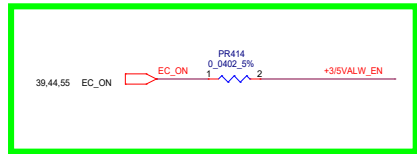
RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL


No charge RTC with 35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)



PR313 PR315 :432K and 64.9k
change to 43k and 7.15k
vin detect volatage level:16.8V
PC309:0.1u change to 0.01u
decrease ACDET deassert time

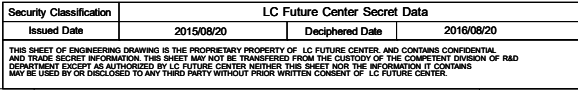
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	PWR-CHARGER
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				Document Number
				DG42A
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				0.1
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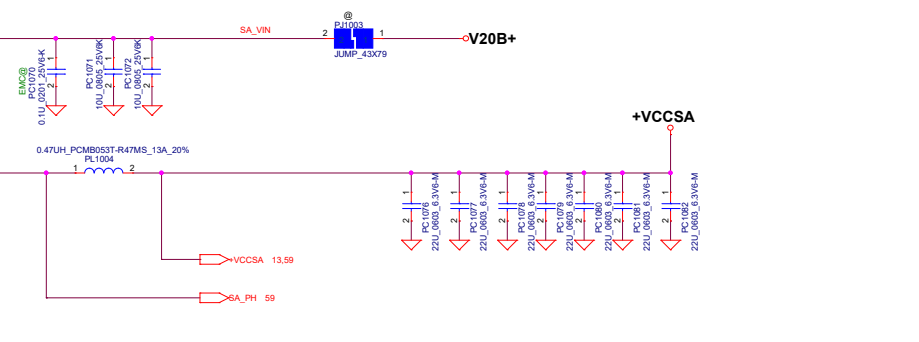
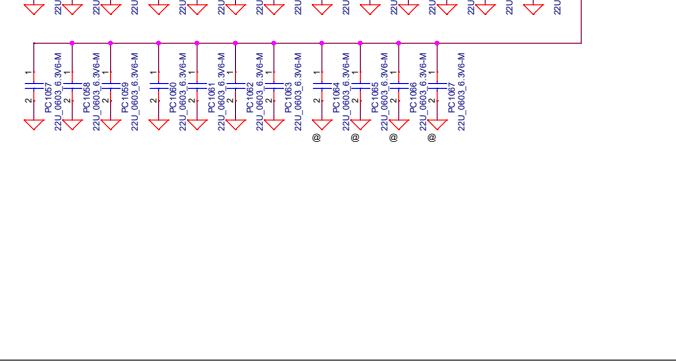
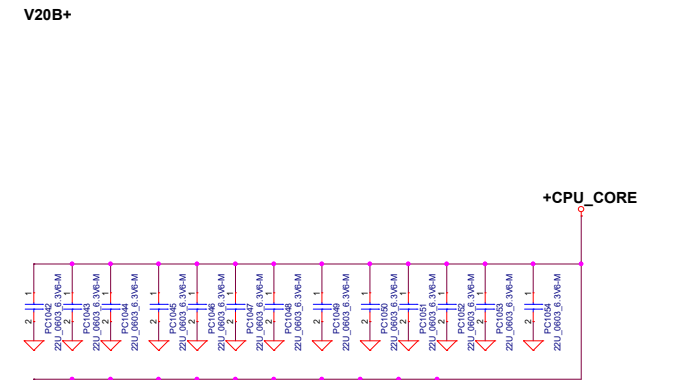
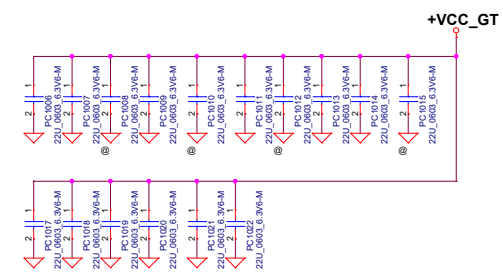



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		5				4				3				2				1			

RVboot	Core	GT	SA
35.7K	0V	0V	1.05V





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2015/08/20		2016/08/20				
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				A2	CG411	0.1
Date:				Thursday, May 04, 2017	Sheet	60 of 60